



**XTX 830**

**Computer-On-Module**

**Reference Manual**

**P/N 5001812BA**

## Preface

This manual provides information about the components, features, connectors and BIOS Setup menus available on the XTX 830. It is one of the documents that should be referred to when designing a Computer-On-Module application. In addition, please refer to the XTX™ Specification.

The links to these documents can be found on the Ampro website at [www.ampro.com](http://www.ampro.com)

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## Intended Audience

This reference manual is intended for technically qualified personnel. It is not intended for general audiences.

## Symbols

The following symbols are used in this reference manual:



### **Warning**

*Warnings indicate conditions that, if not observed, can cause personal injury.*



### **Caution**

*Cautions warn the user about how to prevent damage to hardware or loss of data.*



### **Note**

*Notes call attention to important information that should be observed.*

## Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHZ	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
PCI-EX	PCI Express
SATA	Serial ATA
PATA	Parallel ATA
T.O.M.	Top of memory = max. DRAM installed
HDA	High Definition Audio
I/F	Interface
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

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## XTX™ Concept

The XTX™ concept is an off the shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific

baseboard. XTX modules have a standardized form factor of just 95mm x 114mm and have identical pinouts on the four system connectors. The XTX module provides most of the functional requirements for any application. These functions include, but are not limited to, graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the baseboard interface and carry all the I/O signals to and from the XTX module.

## **XTX Preface from Specification**

Baseboard designers can utilize as little or as many of the I/O interfaces as deemed necessary. The baseboard can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly XTX applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class XTX modules. Simply unplug one module and replace it with another, no redesign is necessary.

## **Lead-Free Designs (RoHS)**

As of July 2006, all electronic products are required to be environmentally friendly. In the future, many of the currently available embedded computer modules will not be offered as lead-free variants. For this reason, all Ampro designs are created from lead-free components and are completely RoHS compliant. This makes Ampro products ideal lead-free substitutes for new and existing designs.

# Contents

1	Specifications .....	1
1.1	Feature List .....	1
1.2	Supported Operating Systems .....	3
1.3	Mechanical Dimensions .....	3
1.4	Supply Voltage Standard Power.....	3
1.4.1	XTX 830 Intel® Core™ Duo L2400 1.66GHz 2MB cache.....	4
1.4.2	XTX 830 Intel® Celeron M M440 1.86GHz 1MB cache .....	5
1.5	Supply Voltage Battery Power.....	5
1.5.1	CMOS Battery Power Consumption.....	5
1.6	Environmental Specifications .....	5
2	Block Diagram.....	6
3	Heatspreader .....	7
3.1	Heatspreader Dimensions.....	8
3.2	Exploded view of Threaded ETX Heatspreader, Module and Carrier Board Assembly .....	9
4	Connector Subsystems.....	10
4.1	Connector X1.....	10
4.1.1	PCI Bus .....	10
4.1.2	USB.....	10
4.1.3	Audio .....	11
4.1.4	Onboard Generated Supply Voltage .....	11
4.2	Connector X2.....	12
4.2.1	LPC .....	12
4.2.2	USB 2.0.....	12
4.2.3	Serial ATA™ .....	12
4.2.4	PCI Express™ .....	12
4.2.5	ExpressCard™ .....	12
4.2.6	AC'97 / HDA (High Definition Audio) Digital Audio.....	13
4.2.7	Extended System Management .....	13
4.3	Connector X3.....	14
4.3.1	Graphics.....	14
4.3.2	LCD .....	14
4.3.3	TV-Out.....	14
4.3.4	Serial Ports (1 and 2) .....	14
4.3.5	Serial Infrared Interface.....	14
4.3.6	Parallel Port/Floppy Interface .....	14
4.3.7	Keyboard/Mouse .....	14
4.4	Connector X4.....	15
4.4.1	IDE .....	15
4.4.2	Ethernet.....	15
4.4.3	I <sup>2</sup> C Bus 400kHz.....	15
4.4.4	Power Control .....	15
4.4.5	Power Management .....	17
5	Additional Features .....	18
5.1	Watchdog .....	18
5.2	Onboard Microcontroller.....	18
5.3	Embedded BIOS .....	18
5.4	SDVO .....	19
5.5	Security Features .....	19
5.6	Suspend to RAM (S3).....	19
6	Tech Notes.....	20
6.1	Comparison of I/O APIC to 8259 PIC Interrupt mode.....	20
6.2	Native vs. compatible IDE mode .....	20
6.2.1	Compatible Mode .....	20

6.2.2	Native Mode .....	20
6.3	Thermal Monitor and Catastrophic Thermal Protection.....	21
6.4	Processor Performance Control .....	23
6.5	Thermal Management .....	23
6.6	ACPI Suspend Modes and Resume Events.....	25
6.7	USB 2.0 EHCI Host Controller Support.....	27
7	Signal Descriptions and Pinout Tables .....	28
7.1	X1 Connector Signal Descriptions.....	29
7.2	Connector X1 Pinout .....	31
7.3	X2 Connector Signal Descriptions.....	32
7.4	X2 Connector Pinout .....	36
7.5	X3 Connector Signal Descriptions.....	37
7.6	X4 Connector Signal Descriptions.....	42
7.7	X4 Connector Pinout .....	45
7.8	SDVO Connector X6 .....	46
7.9	Boot Strap Signals.....	48
8	System Resources.....	49
8.1	System Memory Map.....	49
8.2	I/O Address Assignment.....	50
8.3	Interrupt Request (IRQ) Lines .....	51
8.4	Direct Memory Access (DMA) Channels.....	53
8.5	PCI Configuration Space Map.....	54
8.6	PCI Interrupt Routing Map.....	54
8.7	PCI Bus Masters .....	56
8.8	I <sup>2</sup> C Bus .....	56
8.9	SM Bus.....	56
9	BIOS Setup Description .....	57
9.1	Entering the BIOS Setup Program .....	57
9.1.1	Boot Selection Popup.....	57
9.1.2	Manufacturer Default Settings.....	57
9.2	Setup Menu and Navigation .....	57
9.3	Main Setup Screen.....	58
9.4	Advanced Setup.....	59
9.4.1	ACPI Configuration Submenu .....	60
9.4.2	PCI Configuration Submenu .....	61
9.4.2.1	PCI IRQ Resource Exclusion Submenu .....	62
9.4.2.2	PCI Interrupt Routing Submenu.....	62
9.4.3	Graphics Configuration Submenu .....	63
9.4.4	CPU Configuration Submenu .....	65
9.4.5	Chipset Configuration Submenu .....	66
9.4.6	I/O Interface Configuration Submenu.....	67
9.4.7	Clock Configuration.....	68
9.4.8	IDE Configuration Submenu .....	68
9.4.8.1	Primary/Secondary IDE Master/Slave Submenu .....	69
9.4.9	USB Configuration Submenu .....	70
9.4.9.1	USB Mass Store Device Configuration Submenu.....	71
9.4.10	Keyboard/Mouse Configuration Submenu.....	71
9.4.11	Remote Access Configuration Submenu.....	72
9.4.12	Hardware Monitoring Submenu .....	73
9.4.13	Watchdog Configuration Submenu.....	74
9.5	Boot Setup.....	75
9.5.1	Boot Device Priority.....	75
9.5.2	Boot Settings Configuration .....	76
9.6	Security Setup .....	77
9.6.1	Security Settings .....	77
9.6.2	Hard Disk Security .....	78

9.6.2.1	Hard Disk Security User Password .....	78
9.6.2.2	Hard Disk Security User Password .....	78
9.7	Power Setup .....	79
9.7.1	Exit Menu .....	80
10	Additional BIOS Features.....	81
10.1	Updating the BIOS.....	81
10.2	BIOS Recovery .....	81
10.2.1	BIOS Recovery via Store Devices .....	81
10.2.2	BIOS Recovery via Serial Port .....	82
10.3	Serial Port and Console Redirection.....	82
10.4	BIOS Security Features .....	82
10.5	Hard Disk Security Features .....	83
11	Industry Specifications .....	84

# 1 Specifications

## 1.1 Feature List

**Table 1 Feature Summary**

<b>Form Factor</b>	XTX™ standard (Rev. 1.1)
<b>Processor</b>	Intel® Core™ Duo L2400 1.66GHz, 667MHz with FSB 2-MByte L2 cache LV (Low Voltage) Intel® Celeron M M440 1.86 GHz with 1-MByte L2 cache
<b>Memory</b>	SO-DIMM DDR2 667 up to 2-GByte
<b>Chipset</b>	Graphics and Memory Controller Hub (GMHC) Intel® 82945GM (north bridge) Intel® I/O Controller Hub 82801GBM (ICH7M) (south bridge)
<b>Audio</b>	Realtek ALC 655 AC'97 Rev. 2.2 compatible
<b>Ethernet</b>	ICH7M with PHY Intel® 82562
<b>Graphics Options</b>	<p>Intel® Graphics Media Accelerator 950 with max. 224MByte Dynamic Video Memory Technology (DVMT 3.0) as well as Dual independent display support.</p> <p>CRT Interface 400 MHz RAMDAC Resolutions up to 2048x1536 @ 70Hz (QXGA) including 1920x1080 @ 85Hz (HDTV) Motion Video Support Up-and Downscaling High definition content decode H/W motion compensation Sub picture support Dynamic bob and weave</p> <p>Flat panel Interface (integrated) 2x112MHz LVDS Transmitter Supports all 1x18, 2x18, 1x24, 2x24 Bit TFT configurations (current chipset revisions support 24Bit modes although not officially stated by Intel®) Supports both conventional (FPDI) and non-conventional (LDI) color mappings Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1600x1200 (UXGA)</p> <p>AUX Output 2 x Intel compliant SDVO ports (serial DVO) 200MPixel/sec each Supports external DVI, TV and LVDS transmitter</p> <p>TVOut: Integrated TV encoder Supports component + s-video</p>
<b>Super I/O</b>	Winbond 83627HG
<b>Peripheral Interfaces</b>	<p>2x Serial ATA® I<sup>2</sup>C Bus, Fast Mode (400 kHz) multimaster</p> <p>4 x1 PCI Express® Lanes Floppy (shared with LPT)</p> <p>PCI Bus Rev. 2.0 LPT (EEP/ECP, shared with floppy)</p> <p>6x USB 2.0 (EHCI) 1 x IrDA Port</p> <p>LPC Bus (no ISA Bus) AC'97/HDA (High Definition Audio codecs) Digital Audio interface</p> <p>PS/2 Keyboard, Mouse</p>

<b>BIOS</b>	Based on AMIBIOS8® -1MByte Flash BIOS with Ampro Embedded BIOS features
<b>Power Management</b>	ACPI 2.0 compliant with battery support. Also supports Suspend to RAM (S3)

## 1.2 Supported Operating Systems

- The XTX 830 supports the following operating systems.
- Microsoft® Windows® XP/2000
- Microsoft® Windows® XP Embedded
- Microsoft® Windows® CE 5.0
- Windriver VXWorks®
- Linux®

## 1.3 Mechanical Dimensions

- 95.0 mm x 114.0 mm (3.75" x 4.5")
- Height approx. 12mm (0.4")

## 1.4 Supply Voltage Standard Power

- 5V DC  $\pm$  5%

## Processor Information

In the following power tables there is some additional information about the processors. Intel® offers processors that are considered to be low power consuming. These processors can be identified by their voltage status. Intel uses the following terms to describe these processors. If none of these terms are used then the processor is not considered to be low power consuming.

LV=Low voltage  
ULV=Ultra low voltage

When applicable, the above mentioned terms will be added to the power tables to describe the processor. For example:

Intel® LV Core™ Duo L2400 1.66GHz 2MB L2 cache  
65nm  
Lowest Frequency Mode Min=0.762 Max=1.0  
Highest Frequency Mode Min=1.162 Max=1.3

Intel® also describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables as well. See example below. For information about the manufacturing process visit Intel®'s website.

Intel® LV Core™ Duo L2400 1.66GHz 2MB L2 cache  
65nm  
Lowest Frequency Mode Min=0.762 Max=1.0  
Highest Frequency Mode Min=1.162 Max=1.3

In each processor datasheet, Intel® describes the core voltage (measured in volts V) of the processor. They list either the typical or minimum and maximum core voltage for Lowest Frequency and Highest Frequency Modes depending on the processor. The following terms are used:

Type = Typical core voltage  
 Min = Minimum core voltage  
 Max = Maximum core voltage

This information is also included in the power tables for each processor. For example:  
 Intel® Core™ Duo L2400 1.66GHz 2MB L2 cache  
 LV 65nm  
 Lowest Frequency Mode Min = 0.762 Max = 1.0  
 Highest Frequency Mode Min = 1.162 Max = 1.3

### 1.4.1 XTX 830 Intel® Core™ Duo L2400 1.66GHz 2MB cache

With 512MB memory installed

XTX 830	Intel® Core™ Duo L2400 1.66GHz 2MB L2 cache			
Memory Size	512MB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3)
Power consumption (measured in Amperes/Watts)	1.51/7.55	3.46/17.32	0.69/3.45	0.12/0.61

## 1.4.2 XTX 830 Intel® Celeron M M440 1.86GHz 1MB cache

With 512MB memory installed

<b>XTX 830</b>	Intel® Celeron M M440, 1.86 GHz 1MB L2 cache			
<b>Memory Size</b>	512MB			
<b>Operating System</b>	Windows XP Professional SP2			
<b>Power State</b>	Desktop Idle	100% workload	Standby	Suspend to Ram (S3)
<b>Power consumption (measured in Amperes/Watts)</b>	2.77/13.86	5.08/25.40	1.03/5.16	0.21/1.03

## 1.5 Supply Voltage Battery Power

- 3V DC

### 1.5.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
Integrated in the southbridge	3V DC	2.4 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery life expectancy. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about this, see the Intel® I/O Controller Hub 82801FBM (ICH7M) datasheet.

## 1.6 Environmental Specifications

Temperature	Operation: 0° to 60°C	Store: -20° to +80°C
Humidity	Operation: 10% to 90%	Store: 5% to 95%

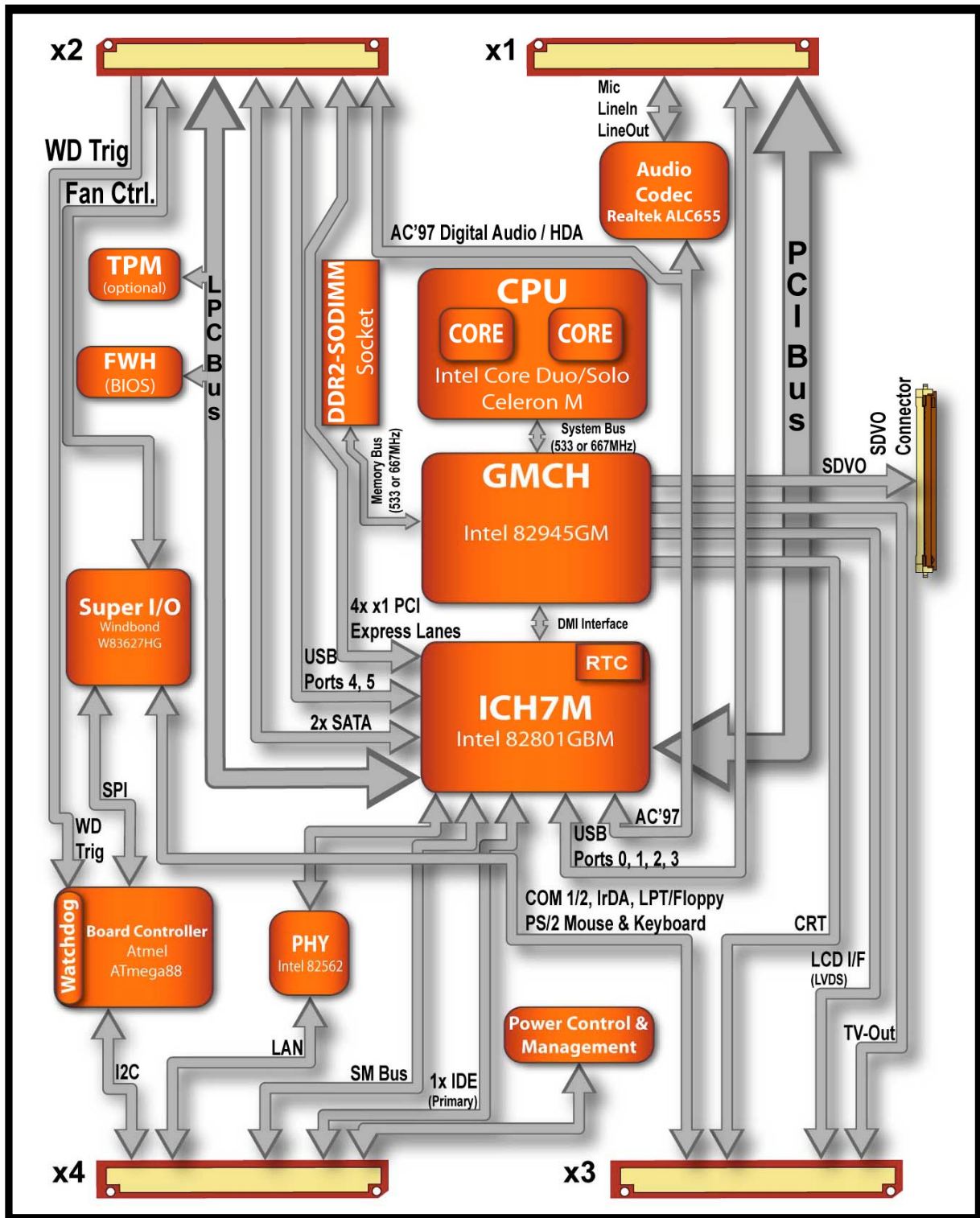


### Note

*The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface. When not using a heatspreader the maximum operating temperature refers to any measurable spot on the module's surface.*

*Humidity specifications are for non-condensing conditions.*

## 2 Block Diagram



## 3 Heatspreader

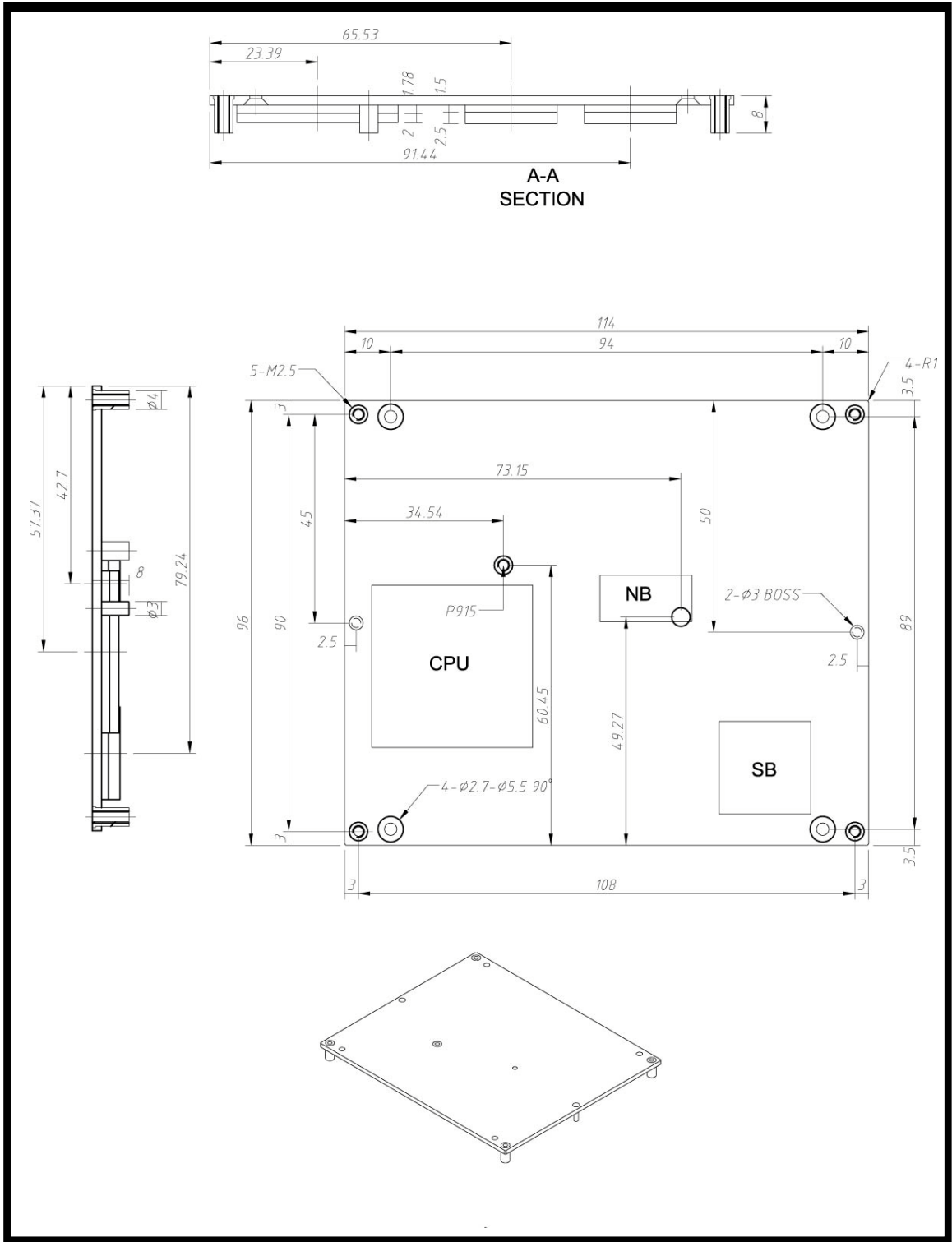
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An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module. It is a 2mm thick aluminum plate. Due to the thickness of the plate all hardware components located beneath the heatspreader should not exceed a height of 6mm. If there are hardware components that do exceed a height of 6mm, then it is possible to implement clearance holes but the mechanical integrity of the heatspreader must be maintained and the components should not exceed a maximum height of 8mm. A heatspreader may also have an access hole so that the memory socket can be accessed when the heatspreader is mounted to the module, but you must ensure that the mechanical integrity of the heatspreader plate is not compromised.

The heatspreader is thermally coupled to the CPU via thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

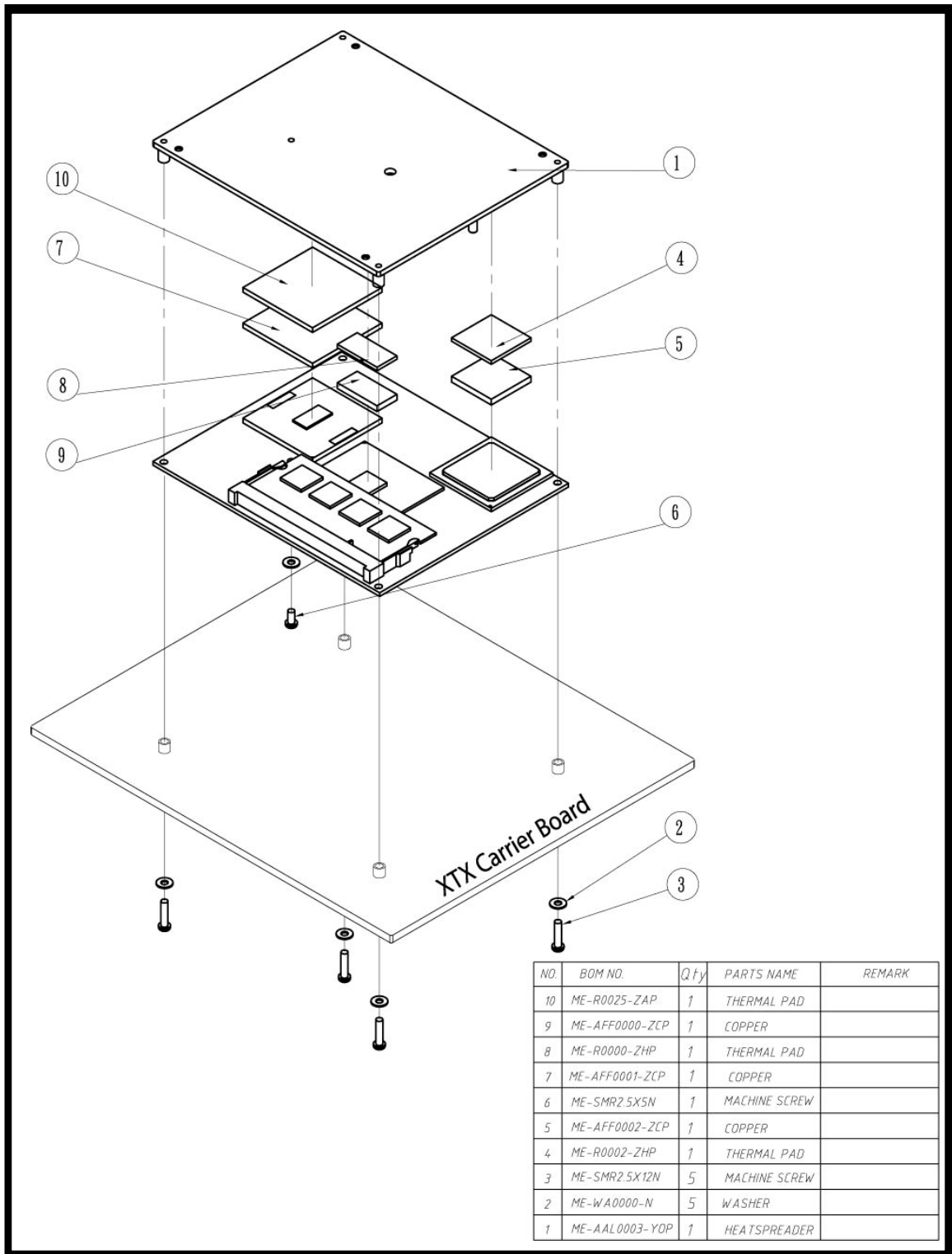
### 3.1 Heatspreader Dimensions



**Note**

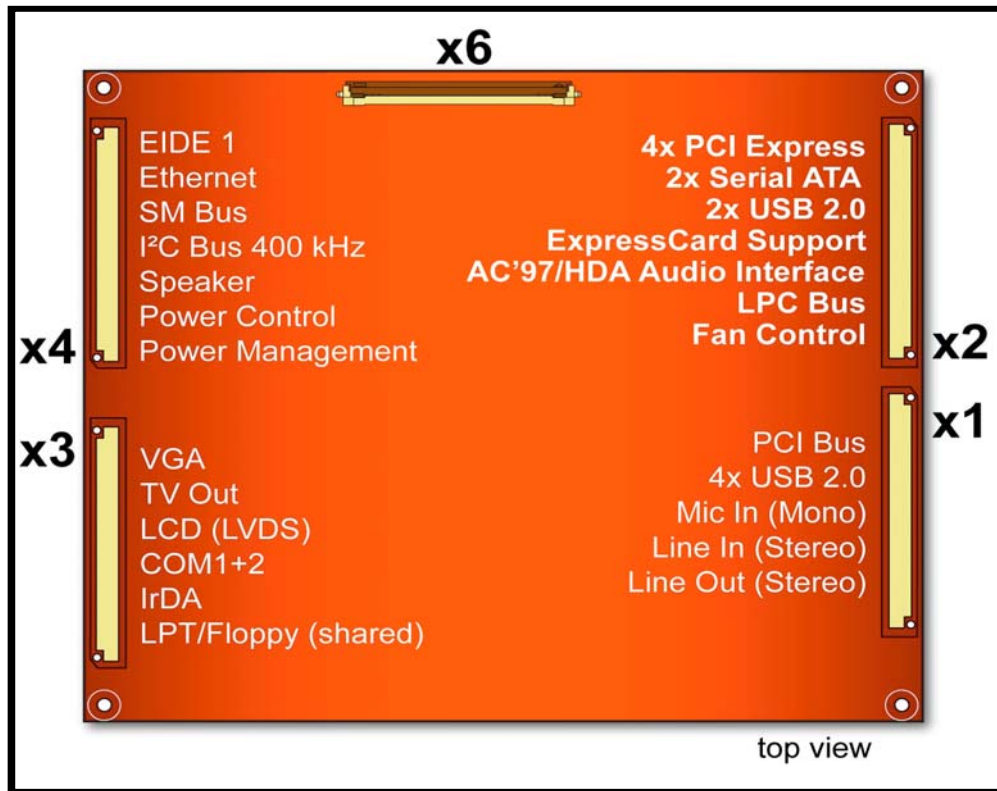
*All measurements are in millimeters.*

### 3.2 Exploded view of Threaded ETX Heatspreader, Module and Carrier Board Assembly



# 4 Connector Subsystems

## X connector Subsystems (top view)



In this view the connectors are seen “through” the module.

### 4.1 Connector X1

The following subsystems can be found on connector X1.

#### 4.1.1 PCI Bus

The implementation of the PCI bus complies with PCI specification Rev. 2.1 and ETX® specification Rev. 2.7

#### 4.1.2 USB

The XTX 830 offers 3 UHCI USB host controllers and one EHCI USB host controller via the Intel® 82801GBM (ICH7M) south bridge. These controllers comply with USB standard 1.1 and 2.0. Four of the six available USB ports are located on the X1 connector. For more information about how the USB host controllers are routed see section 6.7.

### 4.1.3 Audio

The XTX 830 is equipped with a Realtek ALC655 PCI audio controller. It is AC97 2.2 specification compliant and legacy audio SB16™ compatible.



**Note**

The USB and Audio controllers are PCI bus devices. The BIOS allocates the necessary system resources when configuring the PCI devices.

### 4.1.4 Onboard Generated Supply Voltage

Pins 12, 16 and 24 on the X1 connector provide the ability to connect external devices to the modules onboard generated supply voltage ( $3.3V \pm 5\%$ ). 3.3V external devices can be connected to these pins but must not exceed a maximum external load of 500mA. For more information about this feature please contact Ampro technical support.



**Note**

Do not connect pins 12, 16 and 24 to a 3.3V external power supply.

## 4.2 Connector X2

The following subsystems can be found on connector X2.

### 4.2.1 LPC

As a part of the replacement to the no longer supported ISA bus, XTX 830 offers the LPC (Low Pin Count) bus through the use of Intel® 82801GBM (ICH7M) south bridge. There are already many devices available for this Intel defined bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus.

### 4.2.2 USB 2.0

The XTX 830 offers two additional USB ports, via the Intel® 82801GBM (ICH7M) south bridge, that are connected to the X2 connector. These ports are both USB 1.1 and 2.0 compliant. For more information about how the USB host controllers are routed see section 6.7.

### 4.2.3 Serial ATA™

Two Serial ATA150 connections are provided via the Intel® 82801GBM (ICH7M). Serial ATA is an enhancement of the parallel ATA therefore offering higher performance. As a result of this enhancement the traditional restrictions of parallel ATA are overcome with respect to speed and EMV. Serial ATA starts with a transfer rate of 150 Mbytes/s and can be expanded up to 600 Mbytes/s in order to accommodate future developments. Serial ATA is completely protocol and software compatible to parallel ATA.

### 4.2.4 PCI Express™

The XTX 830 offers 4 x1 PCI Express lanes via the Intel® 82801GBM (ICH7M), which can be configured to support PCI Express edge cards or ExpressCards. The PCI Express interface is based on the *PCI Express Specification 1.0a*.

### 4.2.5 ExpressCard™

The XTX 830 supports the implementation of ExpressCards, which requires the dedication of one USB port and one PCI Express lane for each ExpressCard used.

## 4.2.6 AC'97 / HDA (High Definition Audio) Digital Audio

The XTX 830 provides an interface that supports the connection of AC'97 digital audio codecs as well as HDA audio codecs. For more information about this interface consult the XTX Baseboard Application Note.

## 4.2.7 Extended System Management

XTX 830 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN\_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) Output. Additionally there is an input signal called FAN\_TACHOIN that provides the ability to monitor the system fan's RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason a two pulse per revolution fan, or similar hardware solution, is recommended. These features are implemented by the Winbond W83627HG super I/O.

## 4.3 Connector X3

The following subsystems can be found on connector X3. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Please check the BIOS Setup Description section for more information about how to configure a particular subsystem.

### 4.3.1 Graphics

The XTX 830 graphics are driven by an Intel® Graphics Media Accelerator 950 engine, which is incorporated into the Intel® 82945GM chipset found on the XTX 830. This graphic engine offers approximately twice the performance as the Intel® Extreme Graphics Engine found on other Intel® chipsets.

### 4.3.2 LCD

The Intel® 82945GM chipset, found on the XTX 830, offers an integrated dual channel LVDS interface that is connected to Display Pipe B.

### 4.3.3 TV-Out

TV-Out support is integrated into the Intel® 82945GM chipset and is supported on both Display Pipe A and Pipe B.

### 4.3.4 Serial Ports (1 and 2)

The XTX 830 offers two serial interfaces (TTL) that are provided by the I/O controller, which is a Winbond W83627HG super I/O located on the XTX 830.

### 4.3.5 Serial Infrared Interface

Serial port 2 can be configured as a serial infrared interface. The Infrared (IrDA) function provides point-to-point (or multi-point to multi-point) wireless communication, which can operate under various transmission protocols including IrDA SIR. This feature is also implemented by the onboard Winbond W83627HG super I/O.

### 4.3.6 Parallel Port/Floppy Interface

The parallel port/floppy interface can be configured as either a conventional LPT parallel port or a floppy-disk drive port. This is software implemented and can be configured in the BIOS setup program. See section 9.4.6 of this document for information about configuring the parallel port/floppy interface.

### 4.3.7 Keyboard/Mouse

The implementation of these subsystems complies with XTX specification 1.1.

## 4.4 Connector X4

The following subsystems can be found on connector X4. The implementation of all the subsystems complies with ETX® specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Please check the BIOS Setup Description section for more information about how to configure a particular subsystem.

### 4.4.1 IDE

The IDE host adapter is capable of UDMA-100 operation. Only the Primary IDE channel is supported.

### 4.4.2 Ethernet

Ethernet interface is provided by an Intel® 82562 integrated Fast Ethernet NIC controller. The controller is IEEE 802.3u, 10/100Base-Tx fast Ethernet compatible. The interface provides single-ended differential signals that have to be routed through an Ethernet transformer.

### 4.4.3 I<sup>2</sup>C Bus 400kHz

The I<sup>2</sup>C bus is implemented through the use of ATMEL ATmega88 microcontroller. It provides a Fast Mode (400kHz max.) multi-master I<sup>2</sup>C Bus that has maximum I<sup>2</sup>C bandwidth.

### 4.4.4 Power Control

#### PWGIN

PWGIN (pin 4 on the X4 connector) can be connected to an external power good circuit or it may also be utilized as a manual reset input. In order to use PWGIN as a manual reset the pin must be grounded through the use of a momentary-contact pushbutton switch. When external circuitry asserts this signal, it's necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies the XTX 830 module is capable of generating its own power-on reset.

The XTX 830 provides support for controlling ATX-style power supplies. In order to do this the power supply must provide a constant source of 5V power. When not using an ATX power supply then the XTX 830's pins PS\_ON, 5V\_SB, and PWRBTN# should be left unconnected.

#### PS\_ON#

The PS\_ON (pin 5 on the X4 connector) signal is an active-low output that turns on the main outputs of an ATX-style power supply. This open-collector signal can be pulled up to the 5V\_SB supply voltage through the use of a 1K resistor. Usually there is a pull-up resistor internally implemented in the power supply itself yet it is also good practice to implement a footprint for the pull-up resistor in the baseboard circuitry.

## PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 7 on the X4 connector) is used to connect to a momentary-contact, active-low pushbutton input while the other terminal on the pushbutton must be connected to ground. This signal is internally pulled up to 5V\_SB using a 4k7 resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

## Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the XTX 830. The remaining necessary voltages are internally generated on the module using onboard power supplies. A baseboard designer should be aware of the following important information when designing a power supply for a XTX 830 application:

- As mentioned earlier in section 4.1.4 the XTX 830 is capable of generating an onboard 3.3V supply with an output current that is limited to 500mA. If an external device requires more than this 500mA limit, then it is necessary to design a 3.3V supply into the baseboard.



### Caution

*It is not possible to connect an external 3.3V supply to the onboard generated 3.3V supply pins on the XTX 830 module. This will cause the current cross-flow and may result in either a system malfunction and/or damage to the external power supply and the module.*

- Sometimes when designing baseboards, baseboard designers choose to fuse power to some external devices such as keyboards or USB devices by using solid-state or polyswitch over current protection devices. This results in the protective devices typically only opening after they pass several times their rated current for long periods of time. When the application power supply is incapable of generating the necessary current needed to open these protective devices it is possible that the application crashes as a result of an external fault and therefore will reduce the applications reliability as well as make a fault diagnosis of the application difficult.
- It has also been noticed that on some occasions problems occur when using a 5V power supply that produces non-monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem does not arise in the application. For more information about this issue please visit [www.formfactors.org](http://www.formfactors.org) and view page 25 of the document "ATX12V Power Supply Design Guide V2.2".

## 4.4.5 Power Management

APM 1.2 compliant. ACPI 2.0 compliant with battery support. Also supports Suspend to RAM (S3).

# 5 Additional Features

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## 5.1 Watchdog

The XTX 830 is equipped with a multistage watchdog. This solution can be triggered by software and external OEM hardware (input pin is pin 48 on the X2 connector called WDTRG#). For more information about the Watchdog feature see the BIOS setup description section 9.4.13 of this document and the Watchdog Timer Application Note on the Ampro website at [www.ampro.com](http://www.ampro.com).

## 5.2 Onboard Microcontroller

The XTX 830 is equipped with an ATMEL Atmega88 microcontroller. This onboard microcontroller plays an important role for most of the Ampro BIOS features. It fully isolates some of the embedded features such as system monitoring or the I<sup>2</sup>C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in standby mode.

## 5.3 Embedded BIOS

The XTX 830 is equipped with Ampro Embedded BIOS and has the following features:

- ACPI Power Management
- ACPI Battery Support
- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Store
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection
- BIOS Setup Data Backup
- Fast Mode I<sup>2</sup>C Bus
- Console Redirection and BIOS Update (flashing BIOS) via Serial Port

## 5.4 SDVO

Two SDVO (Serial Digital Video Output) ports are supported via a connector located on the bottom side of XTX 830. These ports support the connection of external transmitters such as DVI, TV-Out, and LVDS. For more information about the pinout of the connector (X6), see section 7.8 of this document.

## 5.5 Security Features

The XTX 830 can be equipped optionally with a “Trusted Platform Module” (TPM). This TPM includes co-processors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity, and confidence levels.

## 5.6 Suspend to RAM (S3)

The Suspend to RAM feature is available on the XTX 830.

# 6 Tech Notes

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The XTX 830 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this manual as well as some of the setup nodes found in the BIOS Setup Program description section.

## 6.1 Comparison of I/O APIC to 8259 PIC Interrupt mode

I/O APIC (Advanced Programmable Interrupt controller) mode deals with interrupts differently than the 8259 PIC.

The method of interrupt transmission used by APIC mode is implemented by transmitting interrupts through the system bus and they are handled without the requirement of the processor to perform an interrupt acknowledges cycle.

Another difference between I/O APIC and 8259 PIC is the way the interrupt numbers are prioritized. Unlike the 8259 PIC, the I/O APIC interrupt priority is independent of the actual interrupt number.

A major advantage of the I/O APIC found in the chipset of the XTX 830 is that it's able to provide more interrupts, a total of 24 to be exact. It must be mentioned that the APIC is not supported by all operating systems. In order to utilize the APIC mode it must be enabled in the BIOS setup program before the installation of the OS and it only functions in APIC mode. You can find more information about APIC in the IA-32 Intel Architecture Software Developer's Manual, Volume 3 in chapter 8.



### Note

*You must ensure that your operating system supports APIC mode in order to use it.*

## 6.2 Native vs. compatible IDE mode

### 6.2.1 Compatible Mode

When operating in compatible mode, the SATA and PATA (Parallel ATA) controller together need two legacy IRQs (14 and 15) and are unable to share these IRQs with other devices. This is a result of the fact that the SATA and PATA controller emulate legacy IDE controllers that are non-standard extensions of the ISA based IDE controller.

### 6.2.2 Native Mode

Native mode allows the SATA and PATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources, which means it can be configured anywhere within the system. When either the SATA or PATA controller runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system.

Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a short of interrupts when installing devices.



#### Note

*If your operating system supports native mode then Ampro recommends you enable it.*

## 6.3 Thermal Monitor and Catastrophic Thermal Protection

Intel® Core™ Duo and Solo processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel® Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.



#### Note

*The maximum operating temperature for Intel® Core™ Duo and Solo processors is 100°C. TM2 mode is used for Intel® Core™ Duo and Solo processors.*

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. No additional hardware, software, or handling routines is necessary when using Automatic Mode.



#### Note

*To ensure that the TCC is active for only short periods of time thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Core™ Duo and Solo processors datasheet can provide you with more information about this subject.*

THERMTRIP# signal is used by Intel's Intel® Core™ Duo and Solo processors for catastrophic thermal protection. If the processor's silicon reaches a temperature of approximately 125°C then the processor signal THERMTRIP# will go active and the system will automatically shut down to prevent any damage to the processor as a result of overheating. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.



**Note**

*In order for THERMTRIP# to be able to automatically switch off the system it is necessary to use an ATX style power supply.*

## 6.4 Processor Performance Control

Intel® Core™ Duo and Solo processors run at different voltage/frequency states (performance states). Operating systems that support performance control, take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows XP operating system links its processor performance control policy to the power scheme setting found in the control panel option applet.



### Note

*If the “Home/Office” or “Always On” power scheme is selected when using Windows operating systems then the processor will always run at the highest performance state. For more information about this subject please see chapter 8 of the ACPI Specification Revision 2.0c, which can be found at [www.acpi.info](http://www.acpi.info). Also visit Microsoft's website and search for the document called “Windows Native Processor Performance Control”.*

## 6.5 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This result in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The XTX 830 ACPI thermal solution offers three different cooling policies.

- Passive Cooling

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the “passive cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- Active Cooling

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the “active cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the active cooling device.

- Critical Trip Point

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.



### Notes

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- $\Delta P$  is the performance delta
- $T_t$  is the target temperature = critical trip point.
- The two coefficients  $TC1$  and  $TC2$  and the sampling period  $TSP$  are hardware dependent constants. These constants are set to fixed values for the XTX 830:
- $TC1 = 1$
- $TC2 = 5$
- $TSP = 5$  seconds

See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

## 6.6 ACPI Suspend Modes and Resume Events

XTX 830 supports the S1 (POS= Power On Suspend) state and S3 (STR= Save to Ram). For more information about S3 wake events see Table 14. S4 (Save to Disk) is not supported by the BIOS (S4\_BIOS) but it is supported by the following operating systems (S4\_OS= Hibernate):

- Win2K
- WinXP

The following table lists the “Wake Events” that resume the system from both S1 or S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S1-S5.
GPE1#	Only if configured as Lid Switch in the ACPI setup menu. Additionally the lid button has to be activated using the Windows Power Options. The best way to use it is to go to Standby (see note below) on lid button press and wake from Standby (see note below) on lid button release.
GPE2#	Set GPE2 Function node to Sleep Button in the ACPI setup menu or set Resume On Ring to Enabled in the Power setup menu.
Onboard LAN Event	<p>Device driver must be configured for Wake On LAN support. For configuration go to Device Manger, Network Adapters, Intel(R) PRO/100 VE Network Connection and launch properties.</p> <p>Power Management:            Allow this device to bring the computer out of standby.            Advanced-&gt;Wake on LAN Options-&gt;Properties:            Enable PME: Enabled            Wake On Link Settings: Forced            Wake On Settings: Wake on Mic &amp; Directed</p> <p>Using this configuration the system will wake from Standby (see note below) in case a mic packet or a directed packet is sent.            Directed packet: e.g. ping to last IP / MAC address.            If there is no network cable connected to the system when it goes to Standby (see note below) mode, the system will wake from Standby (see note below) as soon as a cable is connected.</p>
SMBALERT#	Wakes unconditionally from S1-S5.
PCI Express WAKE#	Wakes unconditionally from S1-S3.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manger configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	<p>When Standby mode is set to S1, no special action must be taken for a USB Mouse/Keyboard Event to be used as a Wake Event.</p> <p>When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event..            USB Hardware must be powered by standby power source.            Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu.            Under Windows XP add following registry entries:            Add this key:            HKEY_LOCAL_MACHINE\SYSTEM \ Current Control Set \ Services \ USB            Under this key add the following value:            „USBBIOSx“=DWORD:00000000  <i>Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.</i>            Configure USB keyboard/mouse to be able to wake up the system:            In Device Manger look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.  <i>Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.</i></p>
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu.
Watchdog Power Button Event	Wakes unconditionally from S1-S5.
PS/2 Mouse/Keyboard Event	Only can be used as a Wake Event when in S1 mode.

**Note**

*The above list has been verified using a Windows XP SP2 ACPI enabled installation.*

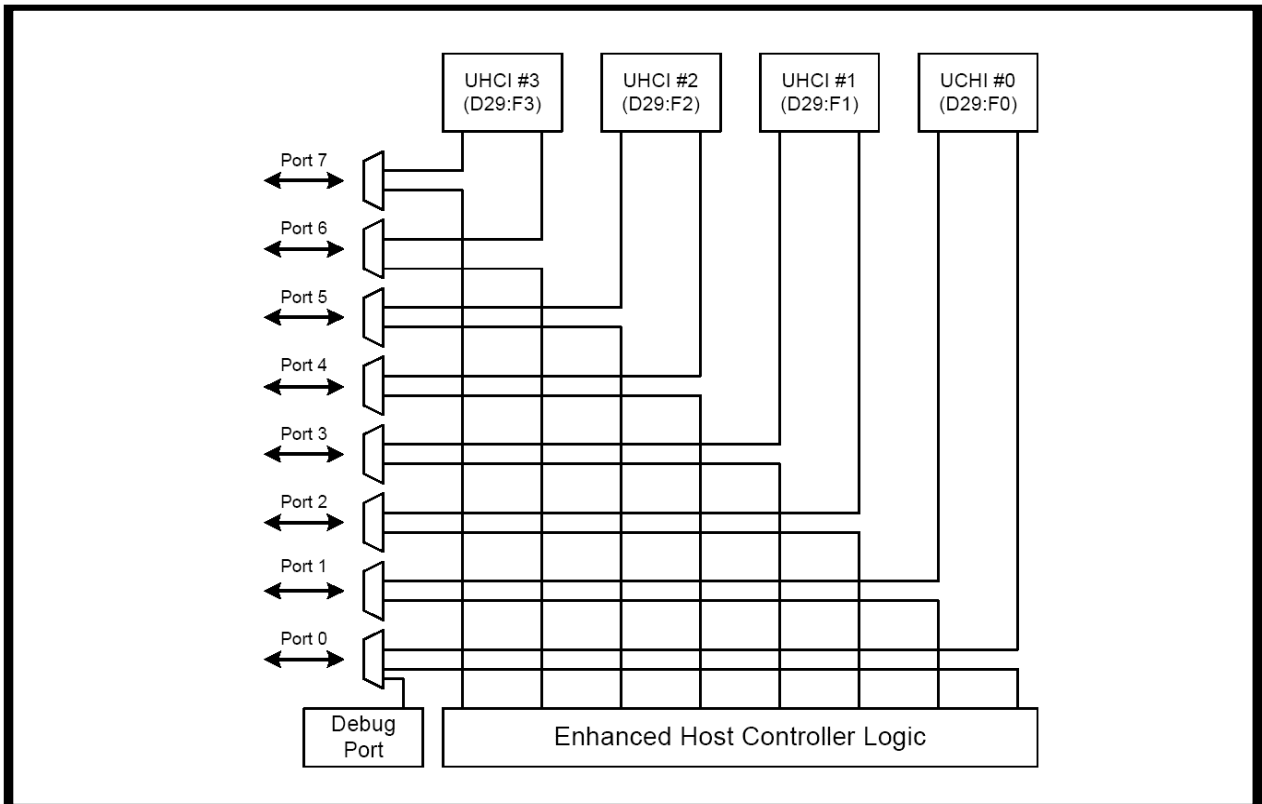
*When using Windows XP, Standby mode is either an S1 state or S3 state depending on what has been selected in the ACPI Configuration Menu in the BIOS setup program. For more information about this, see section 9.4.1 of this document.*

## 6.7 USB 2.0 EHCI Host Controller Support

The 8 USB ports are shared between an EHCI host controller and the 4 UHCI host controllers. Only 6 (USB ports 0-5) of the available 8 USB ports and only 3 (UHCI 0-2) of the available 4 UHCI host controllers are supported on the XTX 830.

Within the EHC functionality there is a port-routing logic that executes the mixing between the two different types of host controllers (EHCI and UHCI). This means that when a USB device is connected the routing logic determines who owns the port. If the device is not USB 2.0 compliant, or if the software drivers for EHCI support are not installed, then the UHCI controller owns the ports.

### Routing Diagram:



# 7 Signal Descriptions and Pinout Tables

The following section describes the signals found on the four X connectors located on the bottom of the module.

This table describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if an internal pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

**Table 2 Signal Tables Terminology Descriptions**

Term	Description
PU	Internally implemented Pull up resistor
PD	Internally implemented Pull down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
SATA	In compliance with Serial ATA specification, Revision 1.0a

## 7.1 X1 Connector Signal Descriptions

**Table 3 Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC ±5%	P		External supply
GND	Power Ground	P		External supply
3V	Power Supply +3.3VDC	P		See section 4.1.4
N.C.	Not Connected	N.A.		Do not connect
SERIRQ	Serial Interrupt request	I 3.3V	PU 10K 3.3V	

**Table 4 PCI Signal Descriptions**

Signal	Description of PCI Bus Signals	I/O	PU/PD	Comment
PCICLK1..4.	Clock output	O 3.3V		
REQ0..3#	Bus request	I 3.3V	PU 8k2 3.3V	REQ1..3# is a boot strap signal (see note below) 5V Tolerant
GNT0..3#	Bus grant	O 3.3V		GNT2/3# is a boot strap signal (see note below)
AD0..31	Address/Data bus lines	I/O 3.3V		5V Tolerant
CBE0..3#	Bus command/byte enables	I/O 3.3V		5V Tolerant
PAR	Bus parity	I/O 3.3V		5V Tolerant
SERR#	Bus system error	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
GPERR#	Bus grant parity error	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
PME#	Bus power management event	I/O 3.3VSB	PU 10k 3.3VSB	
LOCK#	Bus lock	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
DEVSEL#	Bus device select	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
TRDY#	Bus target ready	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
IRDY#	Bus initiator ready	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
STOP#	Bus stop	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
FRAME#	Bus frame	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
PCIRST#	Bus reset	O 3.3V		Asserted during system reset
INTA#	Bus interrupt A	I 3.3V	PU 8k2 3.3V	5V Tolerant
INTB#	Bus interrupt B	I 3.3V	PU 8k2 3.3V	5V Tolerant
INTC#	Bus interrupt C	I 3.3V	PU 8k2 3.3V	5V Tolerant
INTD#	Bus interrupt D	I 3.3V	PU 8k2 3.3V	5V Tolerant



### Note

*Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information please refer to section 7.9 of this manual.*

**Table 5 USB Signal Descriptions**

Signal	Description of USB Signals	I/O	PU/PD	Comment
USB0	USB Port 0, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB0#	USB Port 0, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB1	USB Port 1, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB1#	USB Port 1, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB2	USB Port 2, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USB2#	USB Port 2, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards

USB3	USB Port 3, data + or D+	I/O 3.3V		compatible to USB 1.1 USB 2.0 compliant and backwards compatible to USB 1.1
USB3#	USB Port 3, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1

**Table 6 Audio Signal Descriptions**

Signal	Description of Audio Signals	I/O	PU/PD	Comment
SNDL	Line-Level stereo output left	O		Analog output (1 Vrms)
SNDR	Line-Level stereo output right	O		Analog output (1 Vrms)
AUXAL	Auxiliary input A left	I	22k PD	Analog input (1 Vrms)
AUXAR	Auxiliary input A right	I	22k PD	Analog input (1 Vrms)
MIC	Microphone input	I	2k2 PU AudioVref	Analog input (1 Vrms)
ASGND	Analog ground of sound controller	P		
ASVCC	Analog supply of sound controller	P		5V power output (Can be used as an analog supply for analog amplifier maximum 30mA)

## 7.2 Connector X1 Pinout

Table 7 X1 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCICLK3	4	PCICLK4	53	PAR	54	SERR#
5	GND	6	GND	55	GPERR#	56	Reserved
7	PCICLK1	8	PCICLK2	57	PME#	58	USB2#
9	REQ3#	10	GNT3#	59	LOCK#	60	DEVSEL#
11	GNT2#	12	3V	61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#	63	IRDY#	64	STOP#
15	REQ1#	16	3V	65	FRAME#	66	USB2
17	GNT0#	18	RESERVED	67	GND	68	GND
19	VCC	20	VCC	69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#	71	AD17	72	USB3
23	AD0	24	3V	73	AD19	74	AD18
25	AD1	26	AD2	75	AD20	76	USB0#
27	AD4	28	AD3	77	AD22	78	AD21
29	AD6	30	AD5	79	AD23	80	USB1#
31	CBE0#	32	AD7	81	AD24	82	CBE3#
33	AD8	34	AD9	83	VCC	84	VCC
35	GND	36	GND	85	AD25	86	AD26
37	AD10	38	AUXAL	87	AD28	88	USB0
39	AD11	40	MIC	89	AD27	90	AD29
41	AD12	42	AUXAR	91	AD30	92	USB1
43	AD13	44	ASVCC	93	PCIRST#	94	AD31
45	AD14	46	SNDL	95	INTC#	96	INTD#
47	AD15	48	ASGND	97	INTA#	98	INTB#
49	CBE1#	50	SNDR	99	GND	100	GND

## 7.3 X2 Connector Signal Descriptions

**Table 8 LPC Interface Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
LPC_AD[0..3]	Multiplexed Command, Address and Data.	I/O 3.3V		
LPC_FRAME#	Frame: Indicates start of a new cycle or termination of a broken cycle.	O 3.3V		
LPC_DRQ[0..1]#	Encoded DMA/Bus Master Request.	I 3.3V	PU 10k 3.3V	

**Table 9 Serial ATA Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA0_TX+ SATA0_TX-	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_RX+ SATA1_RX-	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_TX+ SATA1_TX-	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA2_RX+ SATA2_RX-	Serial ATA channel 2, Receive Input differential pair.	N.C.		Not supported
SATA2_TX+ SATA2_TX-	Serial ATA channel 2, Transmit Output differential pair.	N.C.		Not supported
SATA3_RX+ SATA3_RX-	Serial ATA channel 3, Receive Input differential pair.	N.C.		Not supported
SATA3_TX+ SATA3_TX-	Serial ATA channel 3, Transmit Output differential pair.	N.C.		Not supported
IL_SATA#	Serial ATA Interlock Switch Input.	I 3.3V	PU 10k 3.3V	
SATALED#	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V	-	SATALED# is a boot strap signal (see note below)



### Note

*Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information please refer to section 7.9 of this manual.*

**Table 10 PCI Express Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
PCIE0_RX+ PCIE0_RX-	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.0a
PCIE0_TX+ PCIE0_TX-	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.0a
PCIE1_RX+ PCIE1_RX-	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.0a
PCIE1_TX+ PCIE1_TX-	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.0a
PCIE2_RX+ PCIE2_RX-	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.0a
PCIE2_TX+ PCIE2_TX-	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.0a
PCIE3_RX+ PCIE3_RX-	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.0a
PCIE3_TX+ PCIE3_TX-	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.0a
PCIE_CLK_REF+ PCIE_CLK_REF-	PCI Express Reference Clock for Lanes 0 to 3.	O PCIE	PD 49.9R	Please refer to ETX design guide for additional information
PCE_WAKE#	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I 3.3VSB	PU 1k 3.3VSB	

**Table 11 ExpressCard Support Pins Descriptions**

Signal	Description	I/O	PU/PD	Comment
EXEC_CPPE[0..1]#	ExpressCard capable card request.	I 3.3VSB	PU 8k2 3.3VSB	
EXEC_RST[0..1]#	ExpressCard Reset	O 3.3V	PU 10k 3.3V	

**Table 12 Audio Codec Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
AC_RST#	CODEC Reset	O 3.3V		
AC_SYNC	Serial Bus Synchronization.	O 3.3V		AC_SYNC is a boot strap signal (see note below)
AC_BIT_CLK	12.228 MHz Serial Bit Clock from CODEC.	O 3.3V		
AC_SDOOUT	Audio Serial Data Output to CODEC.	O 3.3V		AC_SDOOUT is a boot strap signal (see note below)
AC_SDIN[0..2]	Audio Serial Data Input from CODEC0..CODEC2.	I 3.3V	Only AC_SDIN2 is PD 10k	
CODECSET	Disable onboard Audio Codec.	I 3.3V	PD 10k	

**Note**

*Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information please refer to section 7.9 of this manual.*

**Table 13 USB Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
USBP4	USB Port 4, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USBP4#	USB Port 4, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USBP5	USB Port 5, data + or D+	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1
USBP5#	USB Port 5, data - or D-	I/O 3.3V		USB 2.0 compliant and backwards compatible to USB 1.1

**Table 14 Miscellaneous Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
GND	Ground. All GND pins should be connected to the baseboard ground plane.	P		
5V_SB	Additional Power input for the internal suspend and power-control circuitry. This signal is connected to ETX-Connector X4/Pin3. Refer to ETX Specification for further details.	P		
VCC	5V Power Input. All VCC pins should be connected to the baseboard 5 Volt power plane.	P		
SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	O 3.3VSB	PU 10k 3.3VSB	
SLP_S3#	S3 Sleep Control: This signal shuts off power to all non-critical systems when in S3 (Suspend to Ram), S4 or S5 states.	O 3.3VSB	PU 10k 3.3VSB	
PCI_GNT#A	reserved	O 3.3V		PCI_GNT#A is a boot strap signal (see note below)
PCI_REQ#A	reserved	I 3.3V	PU 8k2 3.3V	
FAN_PWMOUT	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 5V		
FAN_TACHOIN	Fan tachometer input.	I 5V		Requires a fan with a two pulse output.
WDTRIG	Watch Dog Trigger signal.	I 5V	PU 10k 5V	
CLKRUN#	This clock supports the PCI CLKRUN protocol. It connects to peripherals that need to request clock restart or prevention of clock stopping.	I/O 3.3V	PU 8k2 3.3V	
SLP_S5#	SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (soft off) states.	O 3.3VSB	PU 10k 3.3VSB	

## 7.4 X2 Connector Pinout

The following table includes a reference column describing the corresponding standard X2 connector pinout.

**Table 15 X2 Connector Pinout**

Pin	XTX™ Signal	Pin	XTX™ Signal
1	GND	2	GND
3	PCIE_CLK_REF+	4	SATA0_RX+
5	PCIE_CLK_REF-	6	SATA0_RX-
7	GND	8	GND
9	PCIE3_TX+	10	SATA0_TX-
11	PCIE3_TX-	12	SATA0_TX+
13	GND	14	5V_SB
15	PCIE3_RX+	16	SATA1_RX+
17	PCIE3_RX-	18	SATA1_RX-
19	VCC	20	5V_SB
21	EXC1_CPPE#	22	SATA1_TX-
23	EXC1_RST#	24	SATA1_TX+
25	USBP5	26	GND
27	USBP5#	28	SATA2_RX+(*)
29	GND	30	SATA2_RX-(*)
31	PCIE2_TX+	32	SUS_STAT#
33	PCIE2_TX-	34	CLKRUN#
35	GND	36	GND
37	PCIE2_RX+	38	SATA2_TX-(*)
39	PCIE2_RX-	40	SATA2_TX+(*)
41	EXC0_CPPE#	42	GND
43	EXC0_RST#	44	SATA3_RX+(*)
45	USBP4	46	SATA3_RX-(*)
47	USBP4#	48	WDTRIG
49	SLP_S3#	50	SATALED#
51	VCC	52	VCC
53	PCIE1_RX-	54	SATA3_TX-(*)
55	PCIE1_RX+	56	SATA3_TX+(*)
57	GND	58	IL_SATA#
59	PCIE1_TX-	60	RESERVED
61	PCIE1_TX+	62	RESERVED
63	PCE_WAKE#	64	PCI_GNT#A(*)
65	SLP_S5#	66	PCI_REQ#A(*)
67	GND	68	GND
69	PCIE0_RX-	70	RESERVED
71	PCIE0_RX+	72	RESERVED
73	GND	74	VCC
75	PCIE0_TX-	76	RESERVED
77	PCIE0_TX+	78	RESERVED
79	CODECSET	80	VCC
81	AC_RST#	82	AC_SDOUT
83	VCC	84	VCC
85	AC_SYNC	86	AC_SDIN0
87	AC_SDIN1	88	AC_SDIN2
89	AC_BIT_CLK	90	FAN_TACHOIN
91	LPC_AD0	92	FAN_PWMOUT
93	LPC_AD1	94	LPC_FRAME#
95	LPC_AD2	96	LPC_DRQ0#
97	LPC_AD3	98	LPC_DRQ1#
99	GND	100	GND



### Note

The signals marked with an asterisk symbol (\*) are not supported on the XTX 830.

## 7.5 X3 Connector Signal Descriptions

**Table 16 Signal Descriptions**

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC, ±5%	P		External supply
GND	Power Ground	P		External supply
N.C.	Not connected	N.A.		Do not connect
LTGIO0	Not connected	N.C.		Not supported

**Table 17 CRT Signal Descriptions**

Signal	Description of CRT signals	I/O	PU/PD	Comment
HSY	Horizontal Synchronization Pulse	O 3.3V		
VSX	Vertical Synchronization Pulse	O 3.3V		
R	Red channel RGB Analog Video Output	O	PD 150R	Analog output
G	Green channel RGB Analog Video Output	O	PD 150R	Analog output
B	Blue channel RGB Analog Video Output	O	PD 150R	Analog output
DDCK	Display Data Channel Clock	I/O 5V	PU 2k2 5V	
DDDA	Display Data Channel Data	I/O 5V	PU 2k2 5V	

**Table 18 TV Signal Descriptions**

Signal	Description of CRT signals	I/O	PU/PD	Comment
SYNC	Composite sync	N.C.		Not supported
Y	Luminance for S-Video or Red for SCART	O	PD 150R	Analog output
C	Chrominance for S-Video or Green for SCART	O	PD 150R	Analog output
COMP	Composite Video or Blue for SCART	O	PD 150R	Analog output

**Table 19 COM Signal Descriptions**

Signal	Description of COM signals	I/O	PU/PD	Comment
DTR1#	Data terminal ready for COM1	O 5V	PU 4k7 5V	DTR1# is a boot strap signal (see note below)
DTR2#	Data terminal ready for COM2	O 5V	PD 100k 5V	
RI1#, RI2#	Ring indicator for COM1/COM2	I 5V	PD 100k 5V	
TXD1, TXD2	Data transmit for COM1/COM2	O 5V	PU 4k7 5V	TXD1 and TXD2 are boot strap signals (see note below)
RXD1, RXD2	Data receive for COM1/COM2	I 5V	PD 100k 5V	
CTS1#, CTS2#	Clear to send for COM1/COM2	I 5V	PD 100k 5V	
RTS1#	Request to send for COM1	O 5V	PD 4k7	RTS1# is a boot strap signal (see note below)
RTS2#	Request to send for COM2	O 5V	PD 100k 5V	
DCD1#, DCD2#	Data carrier detect for COM1/COM2	I 5V	PD 100k 5V	
DSR1#, DSR2#	Data set ready for COM1/COM2	I 5V	PD 100k 5V	



**Note**

*Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information please refer to section 7.9 of this manual.*

**Table 20 Keyboard and Infrared Signal Descriptions**

Signal	Description of keyboard and infrared signals	I/O	PU/PD
KBDAT	Keyboard Data	I/O 5V	PU 8k2 5V
KBCLK	Keyboard Clock	O 5V	PU 8k2 5V
MSDAT	Mouse Data	I/O 5V	PU 8k2 5V
MSCLK	Mouse Clock	O 5V	PU 8k2 5V
IRTX	Infrared Transmit	O 5V	
IRRX	Infrared Receive	I 5V	

**Table 21 LVDS Flat Panel Signals**

Signal	Description of LVDS Flat Panel signals	I/O	PU/PD	Comment
BIASON	Controls display contrast voltage ON	N.C.		Not supported
DIGON	Controls display Power ON	O 5V	PD 10k	
BLON#	Controls display Backlight ON	O 5V		
LCDDO0..19	LVDS channel data 0..19	O LVDS		
DETECT#	Panel hot-plug detection	N.C.		Not supported
FPDDC_CLK	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
FPDDC_DAT	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

**Table 22 LVDS Interface Pinout**

LVDS Interface Pinout			
Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT#(*)	10	DDDA
11	LCDDO16	12	LCDDO18(*)
13	LCDDO17	14	LCDDO19(*)
15	GND	16	GND
17	LCDDO13	18	LCDDO15
19	LCDDO12	20	LCDDO14
21	GND	22	GND
23	LCDDO8(*)	24	LCDDO11
25	LCDDO9(*)	26	LCDDO10
27	GND	28	GND
29	LCDDO4	30	LCDDO7
31	LCDDO5	32	LCDDO6
33	GND	34	GND
35	LCDDO1	36	LCDDO3
37	LCDDO0	38	LCDDO2
39	VCC	40	VCC
41	FPDDC_DAT	42	LTGIO0
43	FPDDC_CLK	44	BLON#
45	BIASON(*)	46	DIGON
47	COMP	48	Y
49	SYNC(*)	50	C



**Note**

*The signals marked with an asterisk symbol (\*) are not supported on the XTX 830.*

**Table 23 FDC Signal Descriptions**

Signal	Description of FDC signals (shared with LPT)	I/O	Comment
FLPY#	Floppy Interface configuration input	N.A.	Not supported, see section 4.3.6 for more information.
RES	N.C.	N.A.	Not available
DENSEL	Density select: low = 250/300Kb/s high = 500/1000Kb/s	O 5V	
INDEX#	Index signal	I 5V	
TRK0#	Track signal	I 5V	
WP#	Write protect signal	I 5V	
RDATA#	Raw data read	I 5V	
DSKCHG#	Disk change	I 5V	
HDSEL#	Head select	O 5V	
DIR#	Direction	O 5V	
STEP#	Motor step	O 5V	
DRV	Drive select	O 5V	
MOT#	Motor select	O 5V	
WDATA#	Raw write data	O 5V	
WGATE#	Write enable	O 5V	

**Table 24 Floppy Support Mode Pinout**

Floppy Support Mode Pinout			
Pin	Signal	Pin	Signal
51	FLPY# (*)	52	RESERVED
53	VCC	54	GND
55	RESERVED	56	DENSEL
57	RESERVED	58	RESERVED
59	IRRX	60	HDSEL#
61	IRTX	62	RESERVED
63	RXD2	64	DIR#
65	GND	66	GND
67	RTS2#	68	RESERVED
69	DTR2#	70	STEP#
71	DCD2#	72	DSKCHG#
73	DSR2#	74	RDATA#
75	CTS2#	76	WP#
77	TXD2	78	TRK0#
79	RI2#	80	INDEX#
81	VCC	82	VCC
83	RXD1	84	DRV
85	RTS1#	86	MOT
87	DTR1#	88	WDATA#
89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND



**Note**

*The signals marked with an asterisk symbol (\*) are not supported on the XTX 830.*

**Table 25 LPT Signal Descriptions**

Signal	Description of LPT signals (shared with FDC)	I/O	Comment
LPT	LPT Interface configuration input	N.A.	Not supported, see section 4.3.6 for more information.
STB#	Strobe signal	O 5V	
AFD#	Automatic feed	O 5V	
PD0	Data bus D0	I/O 5V	
PD1	Data bus D1	I/O 5V	
PD2	Data bus D2	I/O 5V	
PD3	Data bus D3	I/O 5V	
PD4	Data bus D4	I/O 5V	
PD5	Data bus D5	I/O 5V	
PD6	Data bus D6	I/O 5V	
PD7	Data bus D7	I/O 5V	
ERR#	LPT error	I 5V	
INIT#	Initiate	O 5V	
SLIN#	Select	O 5V	
ACK#	Acknowledge	I 5V	
BUSY	Busy	I 5V	
PE	Paper empty	I 5V	
SLCT	Power On	I 5V	

**Table 26 LPT Support Mode Pinout**

Parallel Port Mode Pinout			
Pin	Signal	Pin	Signal
51	LPT (*)	52	RESERVED
53	VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	VCC	82	VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY
87	DTR1#	88	PE
89	DCD1#	90	SLCT
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND



**Note**

*The signals marked with an asterisk symbol (\*) are not supported on the XTX 830.*

## 7.6 X4 Connector Signal Descriptions

**Table 27 Signal Descriptions**

Signal	Description	I/O	Comment
VCC	Power Supply +5VDC, ±5%	P	External supply
GND	Power Ground	P	External supply
N.C.	Not connected	N.A.	Do not connect
PIDE	Refers to Primary IDE channel	I/O	
SIDE	Refers to Secondary IDE channel	N.C.	Not supported

**Table 28 IDE Signal Descriptions**

Signal	Description of IDE signals	I/O	PU/PD	Comment
PIDE_D0..15	Primary IDE Data bus	I/O 3.3V		5V tolerant
PIDE_A0..2	Primary IDE Address bus	O 3.3V		
PIDE_CS1#	Primary IDE chip select channel 0	O 3.3V		
PIDE_CS3#	Primary IDE chip select channel 1	O 3.3V		
PIDE_DRQ	Primary IDE DMA request	I 3.3V		5V tolerant
PIDED_AK#	Primary IDE DMA acknowledge	O 3.3V		
PIDE_RDY	Primary IDE ready	I 3.3V	PU 4k7 3.3V	5V tolerant
PIDE_IOR#	Primary IDE IO read	O 3.3V		
PIDE_IOW#	Primary IDE IO write	O 3.3V		
PIDE_INTRQ	Primary IDE interrupt request	I 3.3V	PU 8k2 3.3V	5V tolerant
SIDE_D0..15	Secondary IDE Data bus	N.C.		
SIDE_A0..2	Secondary IDE Address bus	N.C.		
SIDE_CS1#	Secondary IDE chip select channel0	N.C.		
SIDE_CS3#	Secondary IDE chip select channel1	N.C.		
SIDE_DRQ	Secondary IDE DMA request	N.C.		
SIDED_AK#	Secondary IDE DMA acknowledge	N.C.		
SIDE_RDY	Secondary IDE ready	N.C.		
SIDE_IOR#	Secondary IDE IO read	N.C.		
SIDE_IOW#	Secondary IDE IO write	N.C.		
SIDE_INTRQ	Secondary IDE interrupt request	N.C.		
DASP_S	Secondary IDE Drive active	N.C.		
PDI_S	Secondary IDE Master/Slave negotiation	N.C.		
HDRST#	Hard Drive reset	O 5V		
CBLID_P#	Not supported	I 3.3V	PD 10k	

**Table 29 Ethernet Signal Descriptions**

Signal	Description of Ethernet signals	I/O	Comment
TXD#, TXD	Ethernet transmit signal pair	O	Signals for external transformer
RXD#, RXD	Ethernet receive signal pair	I	Signals for external transformer
ACTLED#	Ethernet activity LED	O 3.3V	
LILED#	Ethernet link LED	O 3.3V	
SPEEDLED#	Ethernet speed LED, ON at 100Mb/s	O 3.3V	

**Table 30 Power Control Signals**

Signal	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	Power good input	I		Also usable as reset input, make low with O.C. to cause reset.
5V_SB	Supply of internal suspend circuit	P		
PS_ON#	Power Save ON	O 5VSB	PU 10k 5VSB	
PWRBTN#	Power Button	I 5VSB	PU 10k 5VSB	

**Table 31 Power Management Signals**

Signal	Description of Power Management signals	I/O	PU/PD
RSMRST#	Resume / reset input	I 3.3VSB	PU 100k 3.3VSB
SMBALRT#	System management bus alert input	I 3.3VSB	PU 10k 3.3VSB
BATLOW#	Battery low input	I 3.3VSB	PU 10k 3.3VSB
GPE1#	General purpose power management event input 1	I 3.3VSB	PU 10k 3.3VSB
GPE2#	General purpose power management event input 2	I 3.3VSB	PU 10k 3.3VSB
EXTSMI#	System management interrupt input	I 3.3VSB	PU 10k 3.3VSB

**Table 32**      **Miscellaneous Signal Descriptions**

Signal	Description of Miscellaneous signals	I/O	PU/PD	Comment
SPEAKER	Speaker output	O 3.3V		SPEAKER is a boot strap signal (see note below)
BATT	Battery supply	I		
I <sup>2</sup> CLK	I <sup>2</sup> C Bus clock	I/O 5V	PU 10k 5V	
I <sup>2</sup> DAT	I <sup>2</sup> C Bus Data	I/O 5V	PU 10k 5V	
SMBCLK	SM Bus clock	I/O 3.3V	PU 2k2 3.3V	
SMBDATA	SM Bus Data	I/O 3.3V	PU 2k2 3.3V	
KBINH#	Keyboard inhibit	I 5V		
OVCR#	Over current detect for USB	I 3.3VSB	PU 10k 3.3VSB	
ROMKBCS#	Do not connect	N.A.		Not available
EXT_PRG	Do not connect	N.A.		Not available
GPCS#	General purpose chip select	N.C.		Not supported

**Note**

*Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information please refer to section 7.9 of this manual.*

## 7.7 X4 Connector Pinout

Table 33 Connector X4 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	SIDE_IOW#(*)	52	PIDE_IOR#
3	5V_SB	4	PWGIN	53	SIDE_DRQ(*)	54	PIDE_IOW#
5	PS_ON#	6	SPEAKER	55	SIDE_D15(*)	56	PIDE_DRQ
7	PWRBTN#	8	BATT	57	SIDE_D0(*)	58	PIDE_D15
9	KBINH#	10	LILED#	59	SIDE_D14(*)	60	PIDE_D0
11	RSMRST#	12	ACTLED#	61	SIDE_D1(*)	62	PIDE_D14
13	ROMKBCS#(*)	14	SPEEDLED#	63	SIDE_D13(*)	64	PIDE_D1
15	EXT_PRG#(*)	16	I2CLK	65	GND	66	GND
17	VCC	18	VCC	67	SIDE_D2(*)	68	PIDE_D13
19	OVCR#	20	GPCS#(*)	69	SIDE_D12(*)	70	PIDE_D2
21	EXTSMI#	22	I2DAT	71	SIDE_D3(*)	72	PIDE_D12
23	SMBCLK	24	SMBDATA	73	SIDE_D11(*)	74	PIDE_D3
25	SIDE_CS3#(*)	26	SMBALRT#	75	SIDE_D4(*)	76	PIDE_D11
27	SIDE_CS1#(*)	28	DASP_S(*)	77	SIDE_D10(*)	78	PIDE_D4
29	SIDE_A2(*)	30	PIDE_CS3#	79	SIDE_D5(*)	80	PIDE_D10
31	SIDE_A0(*)	32	PIDE_CS1#	81	VCC	82	VCC
33	GND	34	GND	83	SIDE_D9(*)	84	PIDE_D5
35	PDI_S(*)	36	PIDE_A2	85	SIDE_D6(*)	86	PIDE_D9
37	SIDE_A1(*)	38	PIDE_A0	87	SIDE_D8(*)	88	PIDE_D6
39	SIDE_INTRQ(*)	40	PIDE_A1	89	GPE2#	90	CBLID_P#
41	BATLOW#	42	GPE1#	91	RXD#	92	PIDE_D8
43	SIDE_AK#(*)	44	PIDE_INTRQ	93	RXD	94	SIDE_D7(*)
45	SIDE_RDY(*)	46	PIDE_AK#	95	TXD#	96	PIDE_D7
47	SIDE_IOR#(*)	48	PIDE_RDY	97	TXD	98	HDRST#
49	VCC	50	VCC	99	GND	100	GND



### Note

The signals marked with an asterisk symbol (\*) are not supported on the XTX 830.

## 7.8 SDVO Connector X6

Connector and flat foil cable information for the SDVO connector (X6) located on the bottom side of the XTX 830.



- Connector type Hirose 0.5mm Pitch Bottom Contact Type  
Order no. FH12-45S-0.5SH (55)
- FFC type 45 positions, 30cm length, 0.5mm pitch both ends opposite sides  
Manufacturer YOUNGSHIN  
Order No. MCAB45x300B05

**Table 34 SDVO Pinout Description**

Pin	Signal	Description	PU/PD
1	GND	Ground	
2	SDVOC_BCLKN	Serial Digital Video C clock complement.	
3	SDVOC_BCLKP	Serial Digital Video C clock.	
4	GND	Ground	
5	SDVOC_GREEN#	Serial Digital Video C green complement.	
6	SDVOC_GREEN	Serial Digital Video C green.	
7	GND	Ground	
8	SDVOB_BCLKN	Serial Digital Video B clock complement .	
9	SDVOB_BCLKP	Serial Digital Video B clock.	
10	GND	Ground	
11	SDVOB_GREEN#	Serial Digital Video B green data complement.	
12	SDVOB_GREEN	Serial Digital Video B green data.	
13	GND	Ground	
14	SDVOC_INT#	Serial Digital Video input interrupt complement.	
15	SDVOC_INT	Serial Digital Video input interrupt.	
16	GND	Ground	
17	SDVOB_INT#	Serial Digital Video input interrupt complement.	
18	SDVOB_INT	Serial Digital Video input interrupt.	
19	GND	Ground	
20	SDVOC_BLUE#	Serial Digital Video C blue complement.	
21	SDVOC_BLUE	Serial Digital Video C blue data.	
22	GND	Ground	
23	SDVOC_RED#	Serial Digital Video C red data complement / alpha complement.	
24	SDVOC_RED	Serial Digital Video C red data / SDVO B alpha.	
25	GND	Ground	
26	SDVOB_BLUE#	Serial Digital Video B blue data complement.	
27	SDVOB_BLUE	Serial Digital Video B blue data.	
28	GND	Ground	
29	SDVOB_RED#	Serial Digital Video B red data complement.	
30	SDVOB_RED	Serial Digital Video B red data.	
31	GND	Ground	
32	SDVO_FLDSTALL#	Serial Digital Video field stall complement.	
33	SDVO_FLDSTALL	Serial Digital Video field stall.	
34	GND	Ground	
35	SDVO_TVCLKIN#	Serial Digital Video TV-Out synchronization clock complement.	
36	SDVO_TVCLKIN	Serial Digital Video TV-Out synchronization clock.	
37	GND	Ground	
38	SDVOCTRL_CLK	I <sup>2</sup> C based control signal (Clock) for SDVO device.	
39	SDVOCTRL_DATA	I <sup>2</sup> C based control signal (Data) for SDVO device.	SDVOCTRL_DATA is a boot strap signal (see note below)
40	PWRGOOD	PWRGOOD signal	PU 10k 3.3V
41	+5V	Power supply +5V	

Pin	Signal	Description	PU/PD
42	+5V	Power supply +5V	
43	+5V	Power supply +5V	
44	SDAOUFP1	Custom	
45	SDAOUFP2	Custom	



### Note

*Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information please refer to section 7.9 of this manual.*

## 7.9 Boot Strap Signals

**Table 35 Boot Strap signal Descriptions**

Signal	Description of Boot Strap Signals	I/O	PU/PD	Comment
REQ1..3#	Bus request	I 3.3V	PU 8k2 3.3V	REQ1..3# is a boot strap signal (see caution statement below)
GNT2/3#	Bus grant		O 3.3V	GNT2/3# is a boot strap signal (see note below)
SATALED#	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V		SATALED# is a boot strap signal (see caution statement below)
PCI_GNT#A	reserved	O 3.3V		PCI_GNT#A is a boot strap signal (see note below)
AC_SYNC	Serial Bus Synchronization.	O 3.3V		AC_SYNC is a boot strap signal (see caution statement below)
AC_SDOUT	Audio Serial Data Output to CODEC.	O 3.3V		AC_SDOUT is a boot strap signal (see caution statement below)
DTR1#	Data terminal ready for COM1	O 5V	PU 4k7 5V	DTR1# is a boot strap signal (see caution statement below)
TXD1, TXD2	Data transmit for COM1/COM2	O 5V	PU 4k7 5V	TXD1 and TXD2 are boot strap signals (see caution statement below)
RTS1#	Request to send for COM1	O 5V	PD 4k7	RTS1# is a boot strap signal (see caution statement below)
SPEAKER	Speaker output	O 3.3V		SPEAKER is a boot strap signal (see caution statement below)
SDVOCTRL_DATA	I <sup>2</sup> C based control signal (Data) for SDVO device.			SDVOCTRL_DATA is a boot strap signal. Pulled high indicates an external SDVO application is present.



### Caution

*The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either ETX™ internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the ETX™ module to malfunction and/or cause irreparable damage to the module.*

*If it is necessary to drive a TTL input (or another input which sources or sinks significant current) that uses the TXD1 signal, a CMOS-input buffer can be inserted in the signal path so that this line is not pulled up or down by external circuitry during system reset.*

# 8 System Resources

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## 8.1 System Memory Map

Table 36 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(TOM-192kB) – TOM	N.A.	192kB	ACPI reclaim, MPS and NVS area **
(TOM-8MB-192kB) – (TOM-192kB)	N.A.	1 or 8MB	VGA frame buffer *
1024kB – (TOM-8MB-192kB)	100000 – N.A.	N.A.	Extended memory
869kB – 1024kB	E0000 - FFFFF	128kB	Runtime BIOS
800kB – 869kB	CC000 - DFFFF	96kB	Upper memory
640kB – 800kB	A0000 - CBFFF	160kB	Video memory and BIOS
639kB – 640kB	9FC00 - 9FFFF	1kB	Extended BIOS data
0 – 639kB	00000 - 9FC00	512kB	Conventional memory



### Note

*T.O.M. = Top of memory = max. DRAM installed*

*\* VGA frame buffer can be reduced to 1MB in setup.*

*\*\* Only if ACPI Aware OS is set to YES in setup.*

## 8.2 I/O Address Assignment

The I/O address assignment of the XTX 830 module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

**Table 37 I/O Address Assignment**

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
0100 - 010F	16 bytes	No	Ampro System Control
0170 - 0177	8 bytes	No	Secondary IDE channel
01F0 - 01F7	8 bytes	No	Primary IDE channels
02F8 - 02FF	8 bytes	Note 1	Serial Port 2 (COM2)
0376	1 byte	No	Secondary IDE channel command port
0377	1 byte	No	Secondary IDE channel status port
0378 - 037F	8 bytes	Note 1	Parallel Port 1 (LPT1)
03B0 - 03DF	16 bytes	No	Video system
03F0 - 03F5	6 bytes	No	Floppy channel 1
03F6	1 byte	No	Primary IDE channel command port
03F7	1 byte	No	Primary IDE channel status port
03F8 - 03FF	8 bytes	Note 1	Serial Port 1 (COM1)
0480 - 04BF	64 bytes	No	Motherboard resources
04D0 - 04D1	2 bytes	No	Motherboard resources
0800 - 087F	128 bytes	No	Motherboard resources
0A00 - 0A0F	16 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0D00 - FFFF		Note 2	PCI / PCI Express bus



### Notes

1. Default, but can be changed to another address range.
2. The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

## 8.3 Interrupt Request (IRQ) Lines

**Table 38**      **IRQ Lines in PIC mode**

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Note 1	Serial Port 2 (COM2) / Generic	IRQ3 via SERIRQ
4	Note 1	Serial Port 1 (COM1) / Generic	IRQ4 via SERIRQ
5	Yes	Not applicable	IRQ5 via SERIRQ
6	Note 1	Floppy Drive Controller / Generic	IRQ6 via SERIRQ
7	Note 1	Parallel Port 1 (LPT1) / Generic	IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	Note 3	SCI / Generic	IRQ9 via SERIRQ
10	Yes	Not applicable	IRQ10 via SERIRQ
11	Yes	Not applicable	IRQ11 via SERIRQ
12	Note 1	PS/2 Mouse / Generic	IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Note 1, 2	IDE Controller 0 (IDE0) / Generic	IRQ14
15	Note 1, 2	IDE Controller 1 (IDE1) / Generic	IRQ15

In PIC mode, the PCI bus interrupt lines can be routed to any free IRQ.



### Notes

Default, but can be changed to another interrupt. If disabled in BIOS setup, resource can be used for another purpose.

If the ATA/IDE configuration is set to enhanced mode in BIOS setup (serial ATA and parallel ATA native mode operation), IRQ14 and 15 are free for PCI/LPC bus.

In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.

**Table 39 IRQ Lines in APIC mode**

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Note 1	Serial Port 2 (COM2) / Generic	IRQ3 via SERIRQ
4	Note 1	Serial Port 1 (COM1) / Generic	IRQ4 via SERIRQ
5	Yes	Not applicable	IRQ5 via SERIRQ
6	Note 1	Floppy Drive Controller / Generic	IRQ6 via SERIRQ
7	Note 1	Parallel Port 1 (LPT1) / Generic	IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	Note 3	Generic	IRQ9 via SERIRQ, option for SCI
10	Yes	Not applicable	IRQ10 via SERIRQ
11	Yes	Not applicable	IRQ11 via SERIRQ
12	Note 1	PS/2 Mouse / Generic	IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Note 1, 2	IDE Controller 0 (IDE0) / Generic	IRQ14
15	Note 1, 2	IDE Controller 1 (IDE1) / Generic	IRQ15
16	No	N.A.	PIRQA, Integrated VGA Controller, PCI Express Root Port 1, Intel High Definition Audio Controller (Azalia)
17	No	N.A.	PIRQB, AC'97 Audio, PCI Express Root Port 2
18	No	N.A.	PIRQC, Parallel ATA Controller in enhanced/native mode, UHCI Host Controller 2, PCI Express Root Port 3
19	No	N.A.	PIRQD, Serial ATA controller in enhanced/native mode, UHCI Host Controller 1, SMBus Controller, PCI Express Root Port 4
20	Yes	N.A.	PIRQE, PCI Bus INTD, onboard LAN Controller, option for SCI
21	Yes	N.A.	PIRQF, PCI Bus INTA
22	Yes	N.A.	PIRQG, PCI Bus INTB
23	Yes	N.A.	PIRQH, PCI Bus INTC, UHCI Host Controller 0, EHCI Host Controller

In APIC mode, the PCI bus interrupt lines are connected with IRQ 20, 21, 22 and 23.



**Notes**

Default but can be changed to another interrupt. If disabled in BIOS setup, resource can be used for another purpose.

If the ATA/IDE configuration is set to enhanced mode in BIOS setup (serial ATA and parallel ATA native mode operation), IRQ14 and 15 are free for PCI/LPC bus. In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.

## 8.4 Direct Memory Access (DMA) Channels

Table 40 DMA Channels

DMA#	Data Width	Available	Description
0	8 bits	Yes	
1	8 bits	Yes	
2	8 bits	Note 1	Floppy Drive Controller
3	8 bits	Note 2	Parallel Port (LPT)
4	16 bits	No	Cascade DMA Controller
5	16 bits	Yes	
6	16 bits	Yes	
7	16 bits	Yes	



### Notes

1. *If the corresponding device is disabled in BIOS setup then the DMA channel can be used by customers' hardware.*
2. *Not available if Parallel Port is used in ECP mode (Enhanced Parallel Port).*

## 8.5 PCI Configuration Space Map

Table 41 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	02h	00h	Internal	VGA Graphics
00h	02h	01h	N.A.	VGA Graphics
00h	1Bh	00h	Internal	Intel High Definition Audio Controller (Azalia)
00h (Note 1)	1Ch	00h	Internal	PCI Express Root Port 1
00h (Note 1)	1Ch	01h	Internal	PCI Express Root Port 2
00h (Note 1)	1Ch	02h	Internal	PCI Express Root Port 3
00h (Note 1)	1Ch	03h	Internal	PCI Express Root Port 4
00h	1Dh	00h	Internal	UHCI Host Controller 0
00h	1Dh	01h	Internal	UHCI Host Controller 1
00h	1Dh	02h	Internal	UHCI Host Controller 2
00h	1Dh	07h	Internal	EHCI Host Controller
00h	1Eh	00h	Internal	PCI to PCI Bridge
00h	1Eh	02h	Internal	AC97 Audio Controller
00h	1Fh	00h	N.A.	PCI to LPC Bridge
00h	1Fh	01h	Internal	Parallel ATA Controller in enhanced mode
00h	1Fh	02h	Internal	Serial ATA Controller in enhanced mode / Parallel ATA and Serial ATA as combined IDE Controller in compatible mode
00h	1Fh	03h	Internal	SMBus Host Controller
01h (Note 1)	00h	xxh	Internal	PCI Express Port 1
02h (Note 1)	00h	xxh	Internal	PCI Express Port 2
03h (Note 1)	00h	xxh	Internal	PCI Express Port 3
04h (Note 1)	00h	xxh	Internal	PCI Express Port 4
05h (Note 1)	08h	00h	Internal	Onboard LAN Controller
05h (Note 1)	03h	xxh	INTA-INTD	PCI Bus Slot 1
05h (Note 1)	04h	xxh	INTA-INTD	PCI Bus Slot 2
05h (Note 1)	05h	xxh	INTA-INTD	PCI Bus Slot 3
05h (Note 1)	06h	xxh	INTA-INTD	PCI Bus Slot 4



### Notes

1. The given bus numbers only apply if all PCI Express Ports are enabled in the BIOS setup. If for example PCI Express Port 2 is disabled then PCI Express Port 3 will be assigned bus number 2 instead of bus number 3, Port 4 will be assigned bus number 3 and the onboard LAN controller as well as the standard PCI slots will be assigned bus number 4. Furthermore, the respective PCI Express Root Port is hidden if the corresponding PCI Express Port is disabled.

## 8.6 PCI Interrupt Routing Map

Table 42 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line <sup>1</sup>	APIC Mode IRQ	VGA	Azalia HDA	UHCI 0	UHCI 1	UHCI 2	EHCI	PATA Native	SM Bus	AC97
A		16	x	x							
B		17									x
C		18					x		x		
D		19				x				x	
E	INTD	20									
F	INTA	21									

G	INTB	22								
H	INTC	23			x			x		

**Table 43 PCI Interrupt Routing Map (continued)**

PIRQ	LAN	SATA Native	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	PCI-EX Root Port 4	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3	PCI-EX Port 4
A			x				x <sup>2</sup>	x <sup>3</sup>	x <sup>4</sup>	x <sup>5</sup>
B				x	x		x <sup>3</sup>	x <sup>4</sup>	x <sup>5</sup>	x <sup>2</sup>
C						x	x <sup>4</sup>	x <sup>5</sup>	x <sup>2</sup>	x <sup>3</sup>
D		x					x <sup>5</sup>	x <sup>2</sup>	x <sup>3</sup>	x <sup>4</sup>
E	x									
F										
G										
H										



**Notes**

- <sup>1</sup> These interrupts are available for external devices/slots on the X1 connector.
- <sup>2</sup> Interrupt used by single function PCI Express devices (INTA).
- <sup>3</sup> Interrupt used by multifunction PCI Express devices (INTB).
- <sup>4</sup> Interrupt used by multifunction PCI Express devices (INTC).
- <sup>5</sup> Interrupt used by multifunction PCI Express devices (INTD).

## 8.7 PCI Bus Masters

The XTX 830 supports 4 external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.



### Note

*If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.*

## 8.8 I<sup>2</sup>C Bus

There are no onboard resources connected to the I<sup>2</sup>C bus. Address 16h is reserved for Ampro Battery Management solutions.

## 8.9 SM Bus

System Management (SM) bus signals are connected to the Intel® ICH4 82801DB southbridge and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject please contact Ampro technical support.

# 9 BIOS Setup Description

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The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

## 9.1 Entering the BIOS Setup Program

The BIOS setup program can be accessed by pressing the <DEL> key during POST.

### 9.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used a message will be displayed during POST stating that the “Boot Selection Popup menu has been selected” and the menu itself will be displayed immediately after POST thereby allowing the operator to choose the boot device to be used.

### 9.1.2 Manufacturer Default Settings

Pressing the <End> key repeatedly, immediately after power is initiated will result in the manufacturer default settings being loaded. This is helpful when a previous BIOS setting is no longer desired.

## 9.2 Setup Menu and Navigation

The Ampro BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:



### Note

*Entries in the option column that are displayed in bold print indicate BIOS default values.*

Main	Advanced	Boot	Security	Power	Exit
------	----------	------	----------	-------	------

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description	
← →	Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓	Up/Down	Select a setup item or sub menu.
+ -	Plus/Minus	Change the field value of a particular setup item.
Tab		Select setup fields (e.g. in date and time).
F1		Display General Help screen.
F2/F3		Change Colors of setup screen.
F7		Discard Changes.
F9		Load optimal default settings.
F10		Save changes and exit setup.
ESC		Discard changes and exit setup.
ENTER		Display options of a particular setup item or enter submenu.

## 9.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab.

The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
System Time	Hour:Minute:Second	Specifies the current system time. <i>Note: The time is in 24-hour format.</i>
System Date	Day of week, month/day/year	Specifies the current system date. <i>Note: The date is in month-day-year format.</i>
BIOS ID	no option	Displays the BIOS ID.
Processor	no option	Displays the processor type.
System Memory	no option	Displays the total amount of system memory.
Product Revision	no option	Displays the hardware revision of the board
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the Ampro board controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215)
Running Time	no option	Displays the time the board is running [in hours max. 65535].

## 9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Power	Exit
	ACPI Configuration				
	PCI Configuration				
	Graphics Configuration				
	CPU Configuration				
	Chipset Configuration				
	I/O Interface Configuration				
	Clock Configuration				
	IDE Configuration				
	USB Configuration				
	Keyboard/Mouse Configuration				
	Remote Access Configuration				
	Hardware Health Configuration				
	Watchdog Configuration				

## 9.4.1 ACPI Configuration Submenu

Feature	Options	Description
ACPI Aware O/S	No <b>Yes</b>	Set this value to allow the system to utilize the Intel ACPI (Advanced Configuration and Power Interface). Set to <i>NO</i> for non ACPI aware operating system like DOS and Windows NT. Set to <i>YES</i> if your OS complies with the ACPI specification (e.g. Windows 2000, XP)
ACPI APIC support	<b>Enabled</b> Disabled	Set to enable to include the APIC support table to ACPI.
Suspend mode	<b>S1 (POS)</b> S3 (STR)	Select the state used for ACPI system suspends.
USB Device Wakeup From S3/S4	<b>Disabled</b> Enabled	Enable or disable USB device wakeup from S3 and S4 state.
Active Cooling Trip Point	<b>Disabled</b> 50, 60, 70, 80, 90°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Cooling Trip Point	Disabled 50, 60, 70, 80, <b>90</b> °C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Critical Trip Point	Disabled, 80, 85, 90, 95, 100, <b>105</b> , 110°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Watchdog ACPI Event	<b>Shutdown</b> Restart	Select the event that is initiated by the watchdog ACPI event. When the watchdog times out a critical but orderly OS shutdown or restart can be performed (see note below).
GPE1 Function	<b>No Function</b> Lid Switch	Determines the functionality of GPE1 (pin 42 of X4 connector).
GPE2 Function	<b>No Function</b> Sleep Button	Determines functionality of GPE2 (pin 89 of X4 connector).



### Note

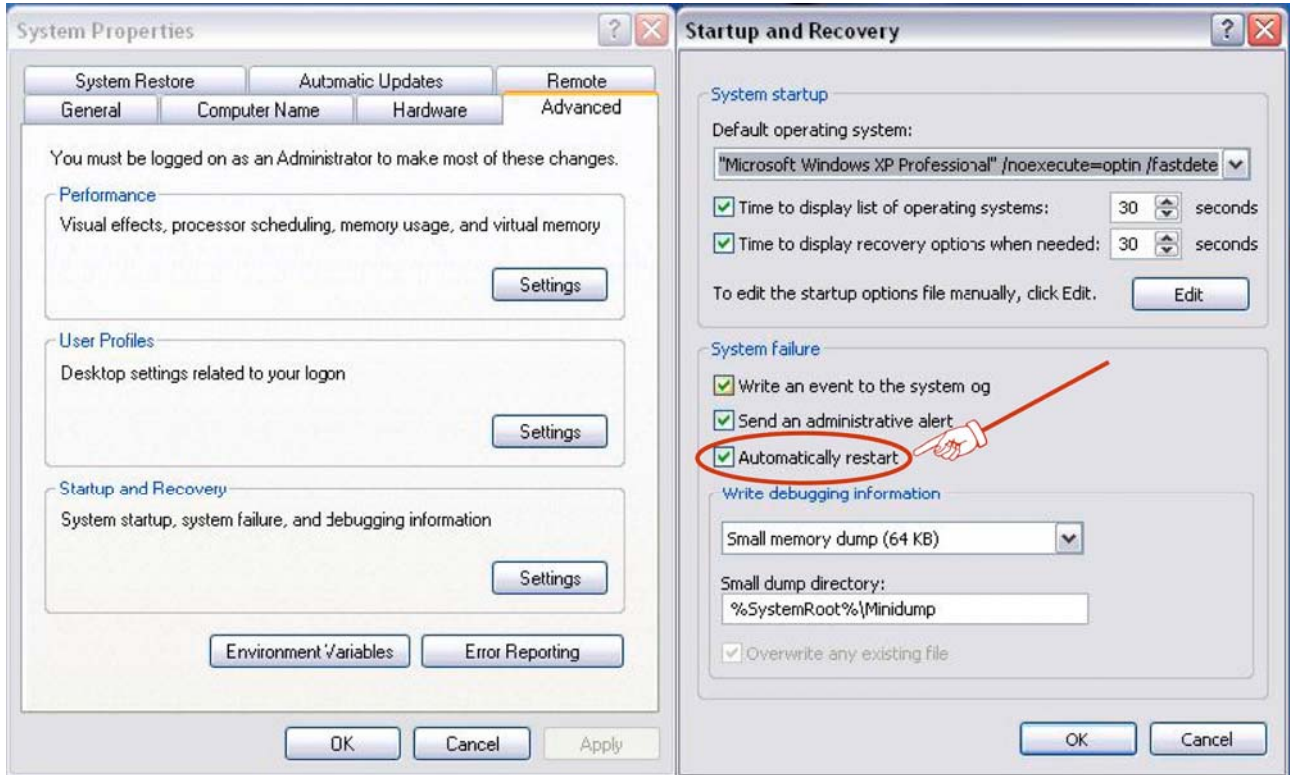
In ACPI mode it is not possible for a “Watchdog ACPI Event” handler to directly restart or shutdown the OS. For this reason the Ampro BIOS will do one of the following:  
For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart.

You can enable this setting by going to the “System Properties” dialog box and choosing the “Advanced” tab. Once there choose the “Settings” button for the “Startup and Recovery” section. This will open the “Startup and Recovery” dialog box. In this dialog box under “System failure” there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event' that is set to 'Restart', you must make sure that the check box for the selection “Automatically restart” has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event' that has been configured for 'Restart' has been generated. Below is a Windows screen-shot showing the proper configuration.

# Win XP/2000 Watchdog ACPI Event restart configuration



## 9.4.2 PCI Configuration Submenu

Feature	Options	Description
Plug & Play O/S	No Yes	Specifies if manual configuration is desired. Set to <i>NO</i> for operating systems that do not meet the Plug and Play specification. In this case the BIOS configure all devices in the system. Select <i>YES</i> to let the operating system configure PnP devices that are not required for booting.
PCI Latency Timer	32, <b>64</b> , 96, ... 248	This option allows you to adjust the latency timer of all devices on the PCI bus.
Allocate IRQ to PCI VGA	Yes No	Allow or restrict the BIOS from giving the VGA controller an IRQ resource.
▶ PCI IRQ Resource Exclusion	sub menu	Opens PCI IRQ Resource Exclusion sub menu.
▶ PCI Interrupt Routing	sub menu	Opens PCI Interrupt Routing sub menu.

### 9.4.2.1 PCI IRQ Resource Exclusion Submenu

Feature	Options	Description
IRQ xx	Available Reserved	Allow or restrict the BIOS from giving IRQ resource to PCI/PNP devices.

### 9.4.2.2 PCI Interrupt Routing Submenu

Feature	Options	Description
PIRQ xx (devices)	Auto, 3, 4, ..., 14, 15	Select fixed IRQ for PCI interrupt line or set to AUTO to let the BIOS and operating system route an IRQ. <i>Note: Make sure that the selected IRQ is not assigned to legacy I/O.</i>

### 9.4.3 Graphics Configuration Submenu

Feature	Options	Description
Primary Video Device	Internal VGA <b>PCI /Int.VGA</b>	Select primary video adapter to be used during boot up.
Internal VGA Mode Select	Disabled Enabled, 1MB <b>Enabled, 8MB</b>	This option allows you to disable the internal VGA controller or enable it with 1MB or 8MB initial frame buffer size.
DVMT Mode Select	Fixed Mode <b>DVMT Mode</b> Combo Mode	Select the DVMT mode to be used by the DVMT graphics driver.  Fixed Mode: The amount of DVMT memory selected is always allocated by the DVMT graphics driver.  DVMT Mode: The DVMT driver only allocates as much memory as required for the current video mode but may allocate memory up to the limit specified in the following node.  Combo Mode: The DVMT graphics driver allocates at least 64MB but may allocate up to 128MB if required.  DVMT = Dynamic Video Memory Technology
DVMT/FIXED Memory	64MB <b>128MB</b>	Amount of DRAM the DVMT graphics driver can or will allocate (depends on DVMT mode selected).
Boot Display Device	Auto CRT only SDVO only CRT + SDVO LFP only <b>CRT + LFP</b>	Select the display device(s) used for boot up. LFP = Local Flat Panel (LVDS)  <i>Note: Auto feature only works with a DDC compatible CRT monitor.</i>
Local Flat Panel Type	<b>Auto</b> VGA 1x18 (002h) VGA 1x18 (013h) SVGA 1x18 (004h) XGA 1x18 (006h) XGA 2x18 (007h) XGA 1x24 (008h) XGA 2x24 (012h) SXGA 2x24 (00Ah) UXGA 2x24 (00Ch) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I <sup>2</sup> C bus. The number in brackets specifies the Ampro internal number of the respective panel data set.  <i>Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.</i>  VGA = 640x480 SVGA = 800x600 XGA = 1024x768 SXGA = 1280x1024 UXGA = 1600x1200
Local Flat Panel Scaling	<b>Centering,</b> Expand Text, Expand Graphics, Expand Text & Graphics	Select whether and how to scale the actual video mode resolution to the local flat panel resolution.
Backlight Control	0%, 25%, 50%, 75%, <b>100%</b>	Set local flat panel backlight control value.
SDVO Port B Device	None <b>DVI</b> TV CRT LVDS	Select the SDVO device connected to this port.
SDVO Port C Device	None <b>DVI</b> TV CRT LVDS	Select the SDVO device connected to this port.
TV Standard	<b>VBIOS-Default</b> NTSC PAL SECAM SMPTE240M ITU-R television	Select TV standard that should be supported. TV connection type is automatically detected by the Video BIOS.

Feature	Options	Description
	SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	
TV Sub-Type	(Options depend on selected TV standard)	Select sub-type for selected TV standard.

## 9.4.4 CPU Configuration Submenu

Feature	Options	Description
Processor Info Block	No option	Displays the processor manufacturer, brand, frequency, and cache sizes.
MPS Revision	1.1 <b>1.4</b>	Select the revision of the multi processor support interface that should be offered by the BIOS. Set back to 1.1 in case problems occur with older non ACPI operating systems.
Max CPUID Value Limit	<b>Disabled</b> Enabled	When <b>enabled</b> , the processor will limit the maximum CPUID input value to <b>03h</b> when queried, even if the processor supports a higher CPUID input value. When <b>disabled</b> , the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Execute Disable Bit	Disabled <b>Enabled</b>	Enable or disable the hardware support for data execution prevention.
Core Multi-Processing	Disabled <b>Enabled</b>	When set to disabled, the second core in a dual core processor system is not used.
Intel SpeedStep tech.	Maximum Speed Minimum Speed <b>Automatic</b> Disabled	Maximum: CPU speed is set to maximum. Minimum: CPU speed is set to minimum. Automatic: CPU speed is controlled by the operating system. Disabled: No SpeedStep, default CPU speed.
Max. CPU Frequency	(Available options depend on processor)	Allows reducing the maximum processor frequency. This limits the maximum frequency the CPU can be set to when SpeedStep is set to Automatic or Maximum Speed.
Intel(R) C-State tech.	Disabled <b>Enabled</b>	Enable or disable advanced CPU C-state support.
C1 Enable	<b>Standard</b> Enhanced	Enable standard or enhanced C1 support.
C2 Enable	Disabled <b>Standard</b> Enhanced	Disable or enable C2 support in standard or enhanced mode.
C3 Enable	Disabled Standard <b>Enhanced</b>	Disable or enable C3 support in standard or enhanced mode.
C4 Enable	Disabled Standard <b>Enhanced</b>	Disable or enable C4 support in standard or enhanced mode.
Hard C4 Enable	Disabled <b>Enabled</b>	Enable or disable hard C4 support (additional power reduction compared to C4).

## 9.4.5 Chipset Configuration Submenu

Feature	Options	Description
Memory Hole	<b>Disabled</b> 15MB-16MB	Enable or disable the memory hole between 15MB and 16MB. If enabled, accesses to this range are forwarded to the LPC / PCI bus.
Chipset Thermal Throttling	<b>Disabled</b> Enabled	This enables or disables Northbridge thermal throttling.
IOAPIC	Disabled <b>Enabled</b>	Enable / Disable ICH7M IOAPIC function.
APIC ACPI SCI IRQ	<b>Disabled</b> Enabled	If set to Disabled IRQ9 is used for the SCI. If set to Enabled IRQ20 is used for the SCI.
C4 On C3	<b>Disabled</b> Enabled	If enabled the CPU is put to C4 state, when the ACPI OS initiates a transition to C3, for additional power saving at "Desktop Idle Mode".
Active State Power Management	<b>Disabled</b> Enabled	Enable or disable PCI Express L0s and L1 link power states.
PCIE Port 0	<b>Enabled</b> Disabled	Enable or disable PCI Express port.
PCIE Port 1	<b>Enabled</b> Disabled	Enable or disable PCI Express port.
PCIE Port 2	<b>Enabled</b> Disabled	Enable or disable PCI Express port.
PCIE Port 3	<b>Enabled</b> Disabled	Enable or disable PCI Express port.
PCIE High Priority Port	<b>Disabled</b> Port 0 Port 1 Port 2 Port 3	Enable PCI Express high priority port for isochronous data transfers.
PCIE Port 0 IOxAPIC Enable	<b>Disabled</b> Enabled	Enable support for IOAPIC behind PCI Express port.
PCIE Port 0 IOxAPIC Enable	<b>Disabled</b> Enabled	Enable support for IOAPIC behind PCI Express port.
PCIE Port 0 IOxAPIC Enable	<b>Disabled</b> Enabled	Enable support for IOAPIC behind PCI Express port.
PCIE Port 0 IOxAPIC Enable	<b>Disabled</b> Enabled	Enable support for IOAPIC behind PCI Express port.

## 9.4.6 I/O Interface Configuration Submenu

Feature	Options	Description
Onboard Audio Controller	Azalia <b>AC97</b> Disabled	Configure onboard audio controller for AC'97 or Azalia (Intel High Definition Audio) mode. <i>Note: Azalia mode requires an external Azalia codec.</i>
Onboard Ethernet Controller	<b>Enabled</b> Disabled	Enable / Disable the ICH7M onboard Ethernet controller.
Onboard Floppy Controller	<b>Disabled</b> Enabled	Enable / Disable the onboard floppy controller.
Floppy A	<b>Disabled</b> 360 KB 5¼" 1.2 MB 5¼" 720 KB 3½" 1.44 MB 3½" 2.88 MB 3½"	Select the floppy drive A type.
Serial Port 1/2 Configuration	Disabled <b>3F8/IRQ4</b> <b>2F8/IRQ3</b> 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 1/2.
Serial Port 2 Mode	<b>Normal</b> IrDA ASK IR	Specifies the mode for serial port 2.
IR Duplex Mode	Full Duplex <b>Half Duplex</b>	Select IRDA full or half duplex function.
IR I/O Pin Select	SINB/SOUTB <b>IRRX/RTX</b>	Select receiver and transmit pins for IRDA mode.
Parallel Port Address	<b>Disabled</b> 378 278 3BC	Specifies the I/O base address used by the parallel port.
Parallel Port Mode	<b>Normal</b> Bi-directional ECP EPP ECP&EPP	Specifies the parallel port mode.
EPP Version	<b>1.9</b> 1.7	Specifies the EPP version.
Parallel Port DMA	DMA0 DMA1 <b>DMA3</b>	Specifies the DMA channel for parallel port in ECP mode.
Parallel Port IRQ	IRQ5 <b>IRQ7</b>	Specifies the interrupt for the parallel port.
Serial Port 3/4 Configuration	<b>Disabled</b> 3F8/IRQ11, 2F8/IRQ10, 3E8/IRQ11, 2E8/IRQ10, 3F8/IRQ10, 2F8/IRQ11, 3E8/IRQ10, 2E8/IRQ11	Specifies the I/O base address and IRQ of serial port 3/4.

## 9.4.7 Clock Configuration

Feature	Options	Description
Spread Spectrum	<b>Disabled</b> Enabled	Enable spread spectrum clock modulation to reduce EMI.

## 9.4.8 IDE Configuration Submenu

Feature	Options	Description
ATA/IDE Configuration	Disabled <b>Compatible</b> Enhanced	Configure the integrated parallel and serial ATA controllers. Disabled: Both controllers are disabled. Compatible: Both controllers operate in legacy or compatible mode. Enhanced: Both controllers operate in enhanced or native mode.
Legacy IDE Channels	SATA Only <b>SATA Pri, PATA Sec</b> PATA Only	Configure the legacy channels in compatible mode.
▶ Primary IDE Master	sub menu	Reports type of connected IDE device.
▶ Primary IDE Slave	sub menu	Reports type of connected IDE device.
▶ Secondary IDE Master	sub menu	Reports type of connected IDE device.
▶ Secondary IDE Slave	sub menu	Reports type of connected IDE device.
Hard Disk Write Protect	<b>Disabled</b> Enabled	If enabled, protects the hard drive from being erased. Disabled allows the hard drive to be used normally. Read, write and erase functions can be performed to the disk.
IDE Detect Time Out (s)	0, 5, 10, ... 30, <b>35</b>	Set this option to stop the BIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing can be found that will allow for all IDE disk drives that are attached to be detected.
ATA(PI) 80Pin Cable Detection	<b>Host &amp; Device</b> Host Device	Select the mechanism for detecting 80Pin ATA (PI) cable. <i>Note: The use of an 80-conductor ATA cable is mandatory for running UDMA66 and faster hard disk drives. The standard 40-conductor ATA cable cannot handle the higher speeds.</i>

### 9.4.8.1 Primary/Secondary IDE Master/Slave Submenu

Feature	Options	Description
Device	Hard Disk ATAPI CDROM	Displays the type of drive detected. The 'grayed-out' items below are the IDE disk drive parameters taken from the firmware of the IDE disk
Vendor	no option	Manufacturer of the device.
Size	no option	Total size of the device.
LBA Mode	supported not supported	Shows whether the device supports Logical Block Addressing.
Block Mode	number of sectors	Block mode boosts IDE performance by increasing the amount of data transferred. Only 512 byte of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 kB per interrupt.
PIO Mode	0, 1, 2, 3, 4	IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.
Async DMA	no option	This indicates the highest Asynchronous DMA Mode that is supported.
Ultra DMA	no option	This indicates the highest Synchronous DMA Mode that is supported.
S.M.A.R.T	no option	Self-Monitoring Analysis and Reporting Technology protocol used by IDE drives of some manufacturers to predict drive failures.
Type	Not Installed <b>Auto</b> CD/DVD ARMD	Sets the type of device that the BIOS attempts to boot from after the POST has completed. <i>Not Installed</i> prevents the BIOS from searching for an IDE disk. <i>Auto</i> allows the BIOS to auto detect the IDE disk drive type. <i>CD/DVD</i> specifies that an IDE CD/DVD drive is attached. The BIOS will not attempt to search for other types of IDE disk drives. <i>ARMD</i> specifies an ATAPI Removable Media Device. This includes, but is not limited to ZIP and LS-120.
LBA/Large Mode	Disabled <b>Auto</b>	Set to <i>AUTO</i> to let the BIOS auto detect LBA mode control. Set to <i>Disabled</i> to prevent the BIOS from using LBA mode.
Block (Multi-Sector Transfer)	Disabled <b>Auto</b>	Set to <i>AUTO</i> to let the BIOS auto detect device support for multi sector transfer. The data transfer to and from the device will occur multiple (the number of sectors, see above) sectors at a time. Set to <i>Disabled</i> to prevent the BIOS from using block mode. The data transfer to and from the device will occur one sector at a time.
PIO Mode	<b>Auto</b> 0, 1, 2, 3, 4	Set to <i>AUTO</i> to let the BIOS auto detect the supported PIO mode.
DMA Mode	<b>Auto</b> SWDMA0, 1, 2 MWDMA0, 1, 2 UDMA0, 1, 2, 3, 4, 5, 6	Set to <i>AUTO</i> to let the BIOS auto detect the supported DMA mode. SWDMA = Single Word DMA MWDMA = Multi Word DMA UDMA = Ultra DMA
S.M.A.R.T	<b>Auto</b> Disabled Enabled	Set to <i>AUTO</i> to let the BIOS auto detect hard disk drive support. Set to <i>Disabled</i> to prevent the BIOS from using SMART feature. Set to <i>Enabled</i> to allow the BIOS to use SMART feature on supported hard disk drives.
32Bit Data Transfer	Disabled <b>Enabled</b>	Enable/Disable 32-bit data transfers on supported hard disk drives.
ARMD Emulation Type	<b>Auto</b> Floppy Hard disk drive	ARMD is a device that uses removable media, such as the LS120, MO (Mneto-optical), or Iomega Zip drives. If you want to boot from media on ARMD, it is required that you emulate boot up from a floppy or hard disk drive. This is essentially necessary when trying to boot to DOS. You can select the type of emulation used if you are booting such a device.

## 9.4.9 USB Configuration Submenu

Feature	Options	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports <b>6 USB Ports</b>	Disable ICH7M USB host controllers. Enable UHCI host controller 0. Enable UHCI host controller 0 + 1. Enable UHCI host controller 0 + 1 + 2.
USB 2.0 Controller	<b>Enabled</b> Disabled	Enable the ICH7M USB 2.0 (EHCI) host controller.
Legacy USB Support	Disabled <b>Enabled</b> Auto	Legacy USB Support refers to the USB keyboard, USB mouse and USB mass store device support. If this option is <i>Disabled</i> , any attached USB device will not become available until a USB compatible operating system is booted. However, legacy support for USB keyboard will be present during POST. When this option is <i>Enabled</i> , those USB devices can control the system even when there is no USB driver loaded. <i>AUTO</i> disables legacy support if no USB devices are connected.
USB Keyboard Legacy Support	Disabled <b>Enabled</b>	Enable/Disable USB keyboard legacy support. <i>NOTE: This option has to be used with caution. If the system is equipped with USB keyboard only then the user cannot enter setup to enable the option back</i>
USB Mouse Legacy Support	Disabled <b>Enabled</b>	Enable/Disable USB mouse legacy support.
USB Store Device Support	Disabled <b>Enabled</b>	Enable/Disable USB mass store device support.
Port 64/60 Emulation	<b>Disabled</b> Enabled	Enable/Disable the "Port 6h/64h" trapping option. Port 60h/64h trapping allows the BIOS to provide full PS/2 based legacy support for USB keyboard and mouse. It provides the PS/2 functionalities like keyboard lock, password setting, scan code selection etc. to USB keyboards.
USB 2.0 Controller Mode	Full Speed <b>HiSpeed</b>	Configures the USB 2.0 host controller in HiSpeed (480Mbps) or Full Speed (12Mbps).
BIOS EHCI Hand-Off	Disabled <b>Enabled</b>	Enable workaround for OSeS without EHCI hand-off support.
USB Beep Message	Disabled <b>Enabled</b>	Enable/Disable the beep during USB device enumeration.
USB Stick Default Emulation	Auto <b>Hard Disk</b>	Select default USB stick emulation type. Auto selects floppy or hard disk emulation based on the store size of the USB stick, but the emulation type can be manually reconfigured for each device using the Mass Store Device Configuration sub menu.
USB Mass Store Reset Delay	10 Sec 20 Sec 30 Sec 40 Sec	Number of seconds the legacy USB support BIOS routine waits for the USB mass store device after the start unit command.
► USB Mass Store Device Configuration	sub menu	Opens sub menu.

### 9.4.9.1 USB Mass Store Device Configuration Submenu

Feature	Options	Description
Emulation Type	<b>Auto</b> Floppy Forced FDD Hard Disk CDROM	Every USB MSD that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. <i>Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.</i> Select <b>AUTO</b> to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. <b>Forced FDD</b> allows a hard disk drive to be connected as a floppy drive. Works only for drives formatted with FAT12, FAT16 or FAT32. <b>Hard Disk</b> allows the device to be emulated as hard disk. <b>CDROM</b> assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

### 9.4.10 Keyboard/Mouse Configuration Submenu

Feature	Options	Description
Bootup Num-Lock	Off <b>On</b>	Specifies the power-on state of the Num-lock feature on the numeric keypad of the keyboard.
Typematic Rate	Slow <b>Fast</b>	Specifies the rate at which the computer repeats a key that is held down. <i>Slow</i> sets a rate of under 8 times per second. <i>Fast</i> sets a rate of over 20 times per second.
PS/2 Mouse Support	Disabled Enabled <b>Auto</b>	<i>Disabled</i> will prevent the PS/2 mouse port from using system resources and will prevent the port from being active. <i>Enabled</i> activates the PS/2 port and the BIOS offers PS/2 mouse support. Use this setting if you always need PS/2 mouse support even when the mouse is not connected at boot-up time. <i>Auto</i> lets the BIOS check for a connected PS/2 mouse and enable support if one is connected.

## 9.4.11 Remote Access Configuration Submenu

Feature	Options	Description
Remote Access	<b>Disabled</b> Enabled	Enable/Disable the BIOS remote access feature. <i>Note: If the systems serial ports are disabled in the 'I/O Interface Configuration' submenu, then Serial Redirection is disabled and 'Remote Access Configuration' menu is unavailable to the users.</i>
Serial Port Number	<b>COM1</b> COM2	Select the serial port you want to use for console redirection. <i>Note: Only enabled serial ports are presented as an option.</i>
Serial Port Mode	<b>115200 8,n,1</b> 57600 8,n,1 19200 8,n,1	Select the baud rate (transmitted bits per second) you want the serial port to use for console redirection. <i>Note: The terminal program used with Serial Redirection must be set to use exact the same set of communication parameters.</i>
Flow Control	<b>None</b> Hardware Software	Select the flow control for Serial Redirection.
Redirection After BIOS POST	Disabled Boot Loader <b>Always</b>	With <i>Disabled</i> Serial Redirection functionality is disabled at the end of BIOS POST. If set to <i>Always</i> , all resources and interrupts associated with Serial Redirection are protected and not released to DOS. This option lets Serial Redirection permanently reside at base memory which allows the DOS console to be redirected. <i>Note, that graphics output (VGA, SVGA, etc) from DOS programs is not redirected!</i> If set to <i>Boot loader</i> , Serial Redirection is active during the OS boot loader process. This allows boot status messages to be redirected, but Serial Redirection will terminate when the OS loads.
Terminal Type	<b>ANSI</b> VT100 VT-UTF8	Select the target terminal type. Escape sequences representing keystrokes are sent to the remote terminal based on these settings.
VT-UTF8 Combination Key Support	Disabled <b>Enabled</b>	This option enables VT-UFT8 combination key support for ANSI/VT100 terminals.
Sredir Memory Display Delay	<b>No Delay</b> Delay 1 Sec Delay 2 Sec Delay 4 Sec	Set the delay in seconds to display memory information if serial redirection is enabled.

## 9.4.12 Hardware Monitoring Submenu

Feature	Options	Description
H/W Health Function	Disabled <b>Enabled</b>	Enable hardware health monitoring device and display the readings.
Board Temperature	no option	Current board temperature.
CPU Temperature	no option	Current processor dies temperature.
Fan1 Speed	no option	Current FAN speed.
VcoreA	no option	Current Core A reading.
VcoreB	no option	Current Core B reading.
+3.3Vin	no option	Current 3.3V reading.
+5Vin	no option	Current 5V reading.
VBAT	no option	Current VBAT reading.

### 9.4.13 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	<b>Disabled</b> 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog.  The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset.
Runtime Watchdog	<b>Disabled</b> One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to ' <i>One time trigger</i> ' the watchdog will be disabled after the first trigger. If set to ' <i>Single event</i> ', every stage will be executed only once, then the watchdog will be disabled. If set to ' <i>Repeated event</i> ' the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	<b>NMI</b> ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about <i>ACPI Event</i> see section 9.4.1 of this manual.
Event 2	<b>Disabled</b> NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	<b>Disabled</b> NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	0.5sec 1sec 2sec 5sec <b>10sec</b> 30sec 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.

## 9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen. In the upper part of the screen the Boot setup allows you to prioritize the available boot devices. The lower part of this setup screen shows options related to the BIOS boot.

### 9.5.1 Boot Device Priority

Feature	Options	Description
Boot Priority Selection	Device Based <b>Type Based</b>	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device  (Up to 12 boot devices can be prioritized if device based priority list control is selected. If "Type Based" priority list control is enabled only 8 boot devices can be prioritized.)	Disabled Primary Master Primary Slave Secondary Master Secondary Slave Legacy Floppy USB Hard disk USB CDROM USB Removable Dev. Onboard LAN External LAN PCI Mass Store PCI SCSI Card Any PCI BEV Device Third Master Third Slave	This view is only available when in the default "Type Based" mode.  When in "Device Based" mode you will only see the devices that are currently connected to the system. The default boot priority is <i>Removable 1st, ATAPI CDROM 2nd, Hard Disk 3rd, BEV 4th</i> (BEV = Boot Entry Vector, e.g. Network or SCSI Option-ROMs).

## 9.5.2 Boot Settings Configuration

Feature	Options	Description
Quick Boot	Disabled <b>Enabled</b>	If <i>Enabled</i> , some POST tasks will be skipped to speed-up the BIOS boot process.
Quiet Boot	<b>Disabled</b> Enabled	<i>Disabled</i> displays normal POST diagnostic messages. <i>Enabled</i> displays OEM logo instead of POST messages. <i>Note: The default OEM logo is a dark screen.</i>
Boot Display	<b>Clear</b> Maintain	Controls the end of POST boot display handling, if Quiet Boot is enabled. If set to <i>Maintain</i> the BIOS will maintain the current display contents and graphics video mode used for POST display. If set to <i>Clear</i> the BIOS will clear the screen and switch to VGA text mode at end of POST.
Automatic Boot List Retry	<b>Disabled</b> Enabled	
Add On ROM Display Mode	<b>Force BIOS</b> Keep current	Set display mode for Option ROM.
Halt On Error	<b>Disabled</b> Enabled	Determines whether the BIOS halt and displays an error message if an error occurs. If set to <i>Enabled</i> the BIOS waits for user input.
Hit 'DEL' Message Display	Disabled <b>Enabled</b>	Allows/Prevents the BIOS to display the ' <i>Hit Del to enter Setup</i> ' message.
Interrupt 19 Capture	<b>Disabled</b> Enabled	Allows/Prevents the option ROMs (such as network controllers) from trapping the boot strap interrupt 19.
PXE Boot to LAN	<b>Disabled</b> Enabled	Disable/Enable PXE boot to LAN <i>Note: When set to 'Enabled', the system has to be rebooted in order for the Intel Boot device to be available in the Boot Device Menu.</i>
Power Loss Control (see note below)	<b>Remain Off</b> Turn On Last State	Specifies the mode of operation if an AC power loss occurs. <i>Remain Off</i> keeps the power off until the power button is pressed. <i>Turn On</i> restores power to the computer. <i>Last State</i> restores the previous power state before power loss occurred. <i>Note: Only works with an ATX type power supply.</i>



### Note

1. The term 'AC power loss' stands for the state when the module loses the standby voltage on the 5V\_SB pins. On Ampro modules, the standby voltage is continuously monitored after the system is turned off. If after 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.
2. Inexpensive ATX power supplies often have problems with short AC power supply. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS\_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.
3. Unlike other module designs available in the embedded market, a CMOS battery is not required by Ampro modules to support the 'Power Loss Control' feature.

## 9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

### 9.6.1 Security Settings

Feature	Options	Description
Supervisor Password	Installed Not Installed	Reports if there is a supervisor password set.
User Password	Installed Not Installed	Reports if there is a user password set.
Change Supervisor Password	enter password	Specifies the supervisor password.
User Access Level	No Access View Only Limited <b>Full Access</b>	Sets BIOS setup utility access rights for user level.
Change User Password	enter password	Specifies the user password.
Password Check	<b>Setup</b> Always	Setup: Check password while invoking setup. Always: Check password also on each boot.
Boot Sector Virus Protection	<b>Disabled</b> Enabled	Select <i>Enabled</i> to enable boot sector protection. The BIOS displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write. <i>Boot Sector Write!</i> <i>Possible VIRUS: Continue (Y/N)?</i> The following appears after any attempt to format any cylinder, head or sector of any hard disk drive via the BIOS INT13 hard disk drive service: <i>Format!!!</i> <i>Possible VIRUS: Continue (Y/N)?</i>

## 9.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

### 9.6.2.1 Hard Disk Security User Password

Feature	Options	Description
Primary/Secondary Master/Slave HDD User Password	enter password	Set or clear the user password for the hard disk. <i>Note: This option will be shaded if the hard drive does support the Security Mode Feature set but user failed to unlock the drive during BIOS POST.</i>

### 9.6.2.2 Hard Disk Security User Password

Feature	Options	Description
Primary/Secondary Master/Slave HDD Master Password	enter password	Set or clear the master password for the hard disk. <i>Note: This option will be shaded if the hard drive does support the Security Mode Feature set but user failed to unlock the drive during BIOS POST.</i>

## 9.7 Power Setup

Select the Power tab from the setup menu to enter the Power Management setup screen.

Feature	Options	Description
Power Management / APM	Disabled <b>Enabled</b>	Set this option to allow or prevent chipset power management and APM (Advanced Power Management).
Suspend Timeout	<b>Disabled</b> 1- 60 Min	Specifies the length of time of inactivity the system waits before it enters suspend mode.
Video Power Down Mode	Disabled Standby <b>Suspend</b>	Specifies the power state that the video subsystem enters when the BIOS places it in a power saving state after the specified period of display inactivity has expired.
Hard Disk Power Down Mode	Disabled Standby <b>Suspend</b>	Specifies the power state that the hard disk drives enter after the specified period of hard drive inactivity has expired.
<Device>	Ignore <b>Monitor</b>	Determines whether the device activity is monitored by the power management timer or not.
Resume On Ring	<b>Disabled</b> Enabled	Disable / enable RI signal (= GPE2 on pin 89 of X4 connector) to generate a wake event. If enabled wake is possible from all power down states including S5 (Soft Off).
Resume On PME	<b>Disabled</b> Enabled	Disable / enable PCI PME to generate a wake event. If enabled wake is possible from all power down states including S5 (Soft Off).
Resume On RTC Alarm	<b>Disabled</b> Enabled	Disable / enable RTC to generate a wake event. If enabled wake is possible from all power down states including S5 (Soft Off).
RTC Alarm Date (Days)	<b>Everyday</b> , 01....31	Select the day of the month when the event should be generated.
System Time	Hour:Minute:Second	Select the system time when the event should be generated.
Power Button Mode	<b>On/Off</b> Suspend	Specifies if the system enters suspend or soft off mode when the power button is pressed.

## 9.7.1 Exit Menu

Select the Exit tab from the setup menu to enter the Exit setup screen.

You can display an Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup and reboot so the new system configuration parameters can take effect.
Discard Changes and Exit	Exit setup without saving any changes made in the BIOS setup program.
Discard Changes	Discard changes without exiting setup. The option values presented when the computer was turned on are used.
Load CMOS Defaults	Load the CMOS defaults of all the setup options.

# 10 Additional BIOS Features

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The XTX 830 uses a Ampro AMI BIOS that is stored in an onboard Flash Rom chip and can be updated using the Ampro System Utility, which is available in a DOS based command line, Win32 command line, and a Win32 GUI version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as X945R1xx, where XTX 830 is the Ampro internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

## 10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS”, please contact Ampro Technical Support Department via email at [info@ampro.com](mailto:info@ampro.com).

## 10.2 BIOS Recovery

The “BIOS recovery” scenario is recommended for situations when the normal flash update fails and the user can no longer boot back to an OS to restore the system. The code that handles BIOS recovery resides in a section of the flash referred to as “boot block”.

For more information about “BIOS Recovery”, please contact Ampro Technical Support Department via email at [info@ampro.com](mailto:info@ampro.com).

### 10.2.1 BIOS Recovery via Store Devices

In order to make a BIOS recovery from a floppy disk, CD-ROM (ISO9660) or USB floppy the BIOS file must be copied into the root directory of the store device and renamed *AMIBOOT.ROM*.

For more information about “BIOS Recovery via Store Devices”, please contact Ampro Technical Support Department via email at [info@ampro.com](mailto:info@ampro.com).

## 10.2.2 BIOS Recovery via Serial Port

The Serial Flash method allows for boot block recovery by loading BIOS via a serial port (COM1). This is can be used by many headless embedded systems which rely on a serial port as a debug and utility console port.

For more information about “BIOS Recovery via Serial Port”, please contact Ampro Technical Support Department via email at [info@ampro.com](mailto:info@ampro.com).

## 10.3 Serial Port and Console Redirection

Serial Redirection allows video and keyboard redirection via a standard RS-232 serial port.

For more information about “Serial Port and Console Redirection”, please contact Ampro Technical Support Department via email at [info@ampro.com](mailto:info@ampro.com).

## 10.4 BIOS Security Features

The BIOS provides both a supervisor and user password. If you use both passwords, the supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when setup is executed. The two passwords activate two different levels of security. If you select password support you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed.

The supervisor password (supervisor mode) gives unrestricted access to view and change all the setup options. The user password (user mode) gives restricted access to view and change setup options.

If only the supervisor password is set, pressing <Enter> at the password prompt of the BIOS setup program allows the user restricted access to setup. Setting the password check to 'Always' restricts who can boot the system. The password prompt will be displayed before the system attempts to load the operating system. If only the supervisor password is set, pressing <Enter> at the password prompt allows the user to boot the system.

## 10.5 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompt the user for the user password. If the user does not enter the correct user password within five attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disable the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

# 11 Industry Specifications

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The list below provides links to industry specifications that apply to Ampro modules.

Specification	Link
Audio Codec '97 Component Specification, Version 2.3 (AC '97)	<a href="http://www.intel.com/design/chipsets/audio/">http://www.intel.com/design/chipsets/audio/</a>
Low Pin Count Interface Specification, Revision 1.0 (LPC)	<a href="http://developer.intel.com/design/chipsets/industry/lpc.htm">http://developer.intel.com/design/chipsets/industry/lpc.htm</a>
Universal Serial Bus (USB) Specification, Revision 2.0	<a href="http://www.usb.org/home">http://www.usb.org/home</a>
PCI Specification, Revision 2.2	<a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>
PCI Express Base Specification, Revision 1.0a	<a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>
Serial ATA Specification, Revision 1.0a	<a href="http://www.serialata.org">http://www.serialata.org</a>
Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003	<a href="http://www.acpi.info">http://www.acpi.info</a>
Information Technology AT Attachment with Packet Interface -5 (ATA/ATAPI-5) Revision 3, February 29, 2000	<a href="http://www.t13.org">http://www.t13.org</a>



