

# CoreModule™/P5e

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P/N 5001481B Revision B



5215 Hellyer Avenue #110, San Jose, CA 95138  
Phone: 408 360-0200, FAX: 408 360-0222, Web: [www.ampro.com](http://www.ampro.com)

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## REVISION HISTORY

<b>Revision</b>	<b>Reason for Change</b>	<b>Date</b>
1/A	Pre-Production Release	5/99
B	Errata Update	8/00
C	Correct Mounting Dimension	10/02

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# Preface

## Introduction

This manual is for integrators and programmers of systems based on the Ampro CoreModule/P5e, a PC/104-Plus CPU module. It contains information about hardware requirements, interconnection, and software configuration.

## Technical Support

Ampro technical support for this product is available from 8:00 AM to 5:00 PM, Pacific time, Monday through Friday. When you call, please have the product's technical manual and the product available.

Table i lists contact information for Ampro technical support.

*Table i. Worldwide Technical Support Contact Information*

Telephone	800-966-5200 (USA), or 408 360-0200
FAX	408 360-0222
Email	techsupport@ampro.com
Website	<a href="http://www.ampro.com">http://www.ampro.com</a>
Surface Mail	Ampro Computers, Incorporated, 4757 Hellyer Avenue, San Jose, CA 95138, USA

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# Chapter 1

## Introduction

### General Description

The CoreModule/P5e is a high integration, high performance Pentium-based PC/AT-compatible system in a PC/104-Plus footprint. This rugged and high quality single-board system is architecturally equivalent to a PC/AT PCI motherboard plus most of the standard PC peripheral interfaces normally needed to create a functioning PC system. Unlike commercial desktop PC motherboards, the CoreModule/P5e is designed to meet the size, power consumption, temperature range, quality, and reliability demands of embedded systems.

Key peripheral functions implemented on the CoreModule/P5e include two buffered serial ports, IrDA port, two Universal Serial Bus (USB) ports, multimode IEEE-1284 parallel port, floppy disk drive controller, PCI-bus EIDE drive controller and standard keyboard, PS/2 mouse, and speaker interfaces. Some versions have an on-board DiskOnChip Flash disk.

The system requires only a single +5 volt power source.

### Ampro Embedded-PC Enhancements

Ampro has made many improvements to the architecture and firmware of the traditional desktop PC to optimize it for embedded applications. The CoreModule/P5e includes a comprehensive set of extensions and enhancements that are specifically designed for embedded systems. Among these are a watchdog timer, serial console, serial boot loader, batteryless boot, failsafe boot, accelerated boot, on-board high-density flash disk, BIOS extensions for OEM boot customization, and comprehensive power-management features.

### Product Feature Summary

- PC/104-Plus Version 1.0-compliant CPU module
- Compact form factor, 0.6 in. x 3.6 in. x 3.8 in.
- Rugged industrial-grade design
- +5 volt-only operation
- Supports PCI and PC/104 expansion busses
- Two 16C550-type serial ports
- IEEE 1284 enhanced parallel port. Supports standard, bi-directional (PS/2), EPP, and ECP modes
- Infrared communications port (IrDA), SIR- and FIR-compliant
- Two Universal Serial Bus (USB) ports
- Standard PC/AT floppy disk controller

- EIDE hard disk controller
    - Fast transfers up to PIO mode 4
    - Supports Ultra DMA/33 transfers
    - LBA mode compatible (supports >512 MB drives)
    - Supports IDE CD-ROM boot
  - Configurable watchdog timer
  - Temperature sensor and CPU speed control for increased reliability
- Serial EEPROM-backed CMOS configuration data - permits battery-free operation

## Enhanced Reliability

Reliability is especially important in embedded computer systems. Ampro, specializing in embedded system computers and peripherals, knows that embedded systems must be able to run reliably in rugged, hostile, and mission-critical environments without operator intervention. Over the years, Ampro has evolved system designs and a comprehensive testing program to ensure a reliable and stable system for harsh and demanding applications. These include:

- ISO 9001 Manufacturing
- Regulatory testing
- Wide-range temperature testing
- Mobile Pentium processor with MMX technology on 0.25 micron
- Shock and Vibration Testing
- HALT Testing

For details about CoreModule/P5e testing, see *Ampro Product Reliability Testing* on page 3-3.

Figure 1-1 is a block diagram of the CoreModule/P5e architecture.

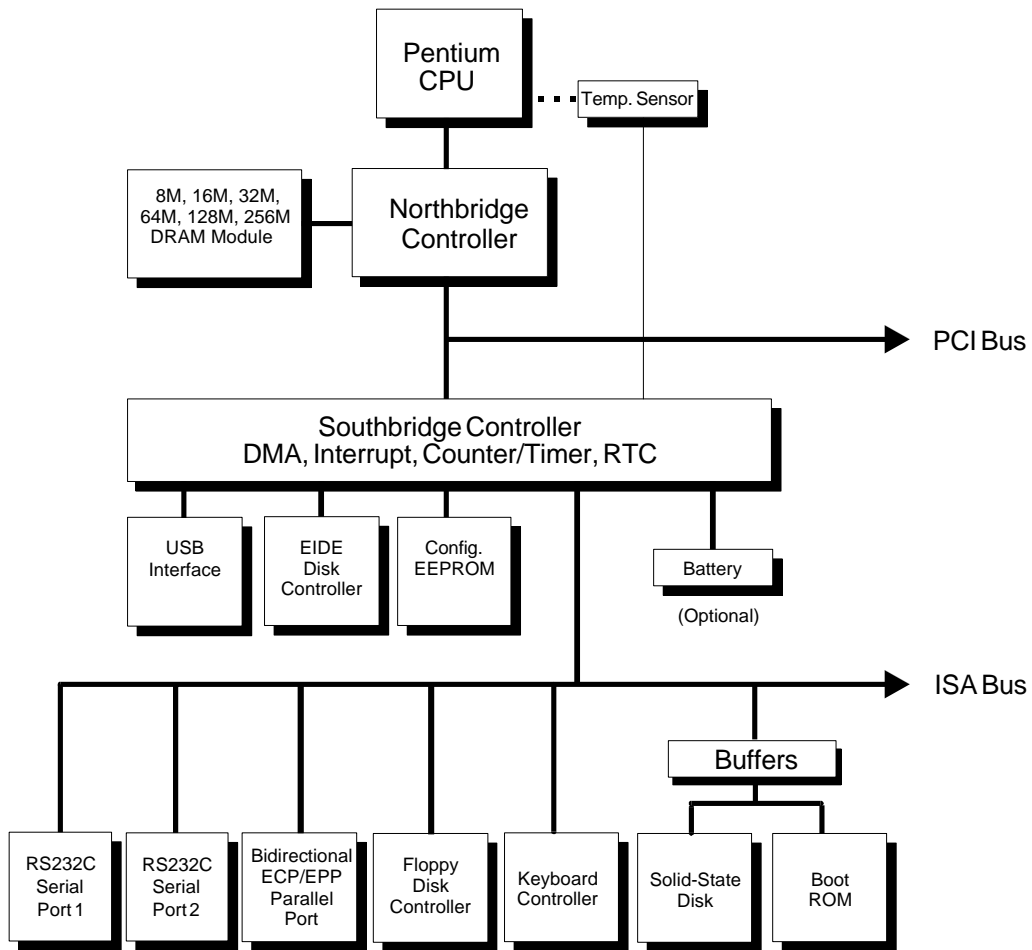


Figure 1-1. System Block Diagram

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# Chapter 2

## Product Reference

### Overview

This chapter contains the technical information you will need to install and configure the CoreModule/P5e. The information is presented in the following order:

- Mounting Dimensions (page 2-2)
- Connector Summary (page 2-3)
- CPU Topics (page 2-6)
- DRAM (page 2-9)
- Power Interface (page 2-11)
- Serial Ports (page 2-14)
- IrDA Port (page 2-19)
- Parallel Port (page 2-20)
- Floppy Interface (page 2-29)
- EIDE Hard Disk Interface (page 2-31)
- Universal Serial Bus (USB) Ports (page 2-34)
- Setup Function (page 2-45)

# Mounting Dimensions

Figure 2-1 shows the CoreModule/P5e mounting dimensions.

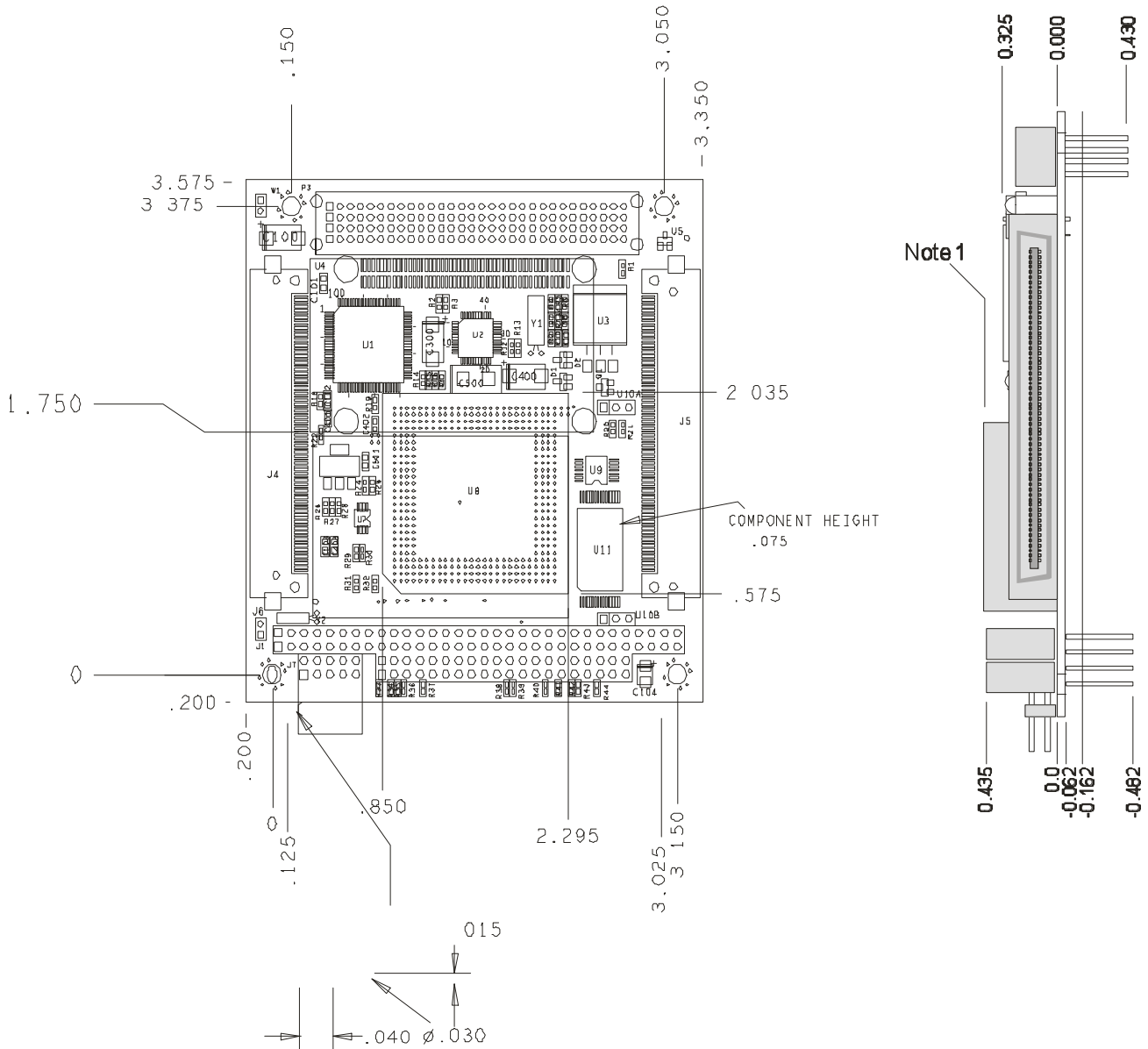


Figure 2-1. Mounting Dimensions

**Note 1:** Height and size of heatsink can vary, depending on what model you select.

## Connector Summary

Table 2-1 summarizes the use of the CoreModule/P5e's I/O connectors. Each interface is described later in its own section, showing connector pinouts, signal definitions, connector descriptions, and key pins, if any.

Table 2– 1. CoreModule/P5e Connector Summary

Connector	Function	Type	Key Pin
P1A,B	PC/104 Bus	64-pin Interboard	B10
P2C,D	PC/104 Bus	40-pin Interboard	C19
P3	PCI Bus	4 x 30 Interboard	A1
J4	I/O Connector: <ul style="list-style-type: none"> <li>■ Floppy</li> <li>■ EIDE</li> </ul>	High-Density 80-Pin, for dual 40-Pin Ribbon Cables	
J5	I/O Connector: <ul style="list-style-type: none"> <li>■ Speaker</li> <li>■ Keyboard</li> <li>■ Mouse</li> <li>■ Reset Switch</li> <li>■ HD Activity LED</li> <li>■ Battery</li> <li>■ Serial 1, Serial 2</li> <li>■ IrDA</li> <li>■ USB1 USB2</li> <li>■ Parallel</li> </ul>	High-Density 80-Pin, for dual 40-Pin Ribbon Cables	
J7	Power	10-Pin	7
J6	Power (1=+5, 2=GND)	2-Pin Latching	

Note: Designators J1, J2, J3, are not used.

## Connectors

The ISA portion of the PC/104-Plus expansion bus appears on two connectors, P1 and P2. You can expand the system with MiniModule products or other PC/104-compliant expansion modules installed in these connectors. P1 and P2 have both male and female connections, allowing you to stack modules or to easily install a module on a custom motherboard. Pinout lists for these connectors are provided on Table 2-24 to Table 2-7.

The PCI portion of the PC/104-Plus expansion bus appears on connector P3. It uses a 2 mm, 4-row connector called out in the PC/104-Plus draft specification. Like the P1/P2 connectors, P3 has both male and female connections, allowing for “stackthrough” assembly or installation on a custom motherboard. Pinout for this connector is provided on Table 2-28.

J4 and J5 are 80-pin high-density shrouded dual-row male headers (Hirose FX2BA-80S-1.27R) for use with flat ribbon (IDC) connectors and ribbon cable. J4 and J5 interface to standard 100 mil 40-conductor ribbon cables, which in turn can be split to provide connection to standard insulation displacement connectors (IDC) for the various peripherals.

A summary of the pinouts of J4 and J5 are shown in Table 2-2 and Table 2-3. These tables give you an at-a-glance view of all the pins on these connectors. Note that the signals are arranged to provide straight-through connection to peripherals via standard IDC connectors. Additional cabling information for each peripheral interface is provided in sections that describe each peripheral. Drawings for typical cables are provided in Appendix A.

Connectors may have “key pins,” as indicated in connector pinout tables. Install a blocking key in the corresponding connector socket on the mating ribbon cable to prevent accidental misalignment when installing the cable.

Table 2– 2. J4 Pinout Summary

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	FPY:Ground	3	FPY:DEN	2	HD:RESET*	4	HD:Ground
5	FPY:Ground	7	FPY:N/C	6	HD:D7	8	HD:D8
9	FPY:Ground	11	FPY:KEY	10	HD:D6	12	HD:D9
13	FPY:Ground	15	FPY:INDX	14	HD:D5	16	HD:D10
17	FPY:Ground	19	FPY:MO0	18	HD:D4	20	HD:D11
21	FPY:Ground	23	FPY:DS1	22	HD:D3	24	HD:D12
25	FPY:Ground	27	FPY:DS0	26	HD:D2	28	HD:D13
29	FPY:Ground	31	FPY:MO1	30	HD:D1	32	HD:D14
33	FPY:Ground	35	FPY:DIR	34	HD:D0	36	HD:D15
37	FPY:Ground	39	FPY:STEP	38	HD:Ground	40	HD:KEY
41	FPY:Ground	43	FPY:WDAT A	42	N/C(DRQ)	44	HD:Ground
45	FPY:Ground	47	FPY:WRGT	46	HD:IOW*	48	HD:Ground
49	FPY:Ground	51	FPY:TR0	50	HD:IOR*	52	HD:Ground
53	FPY:Ground	55	FPY:WPRT	54	IORDY	56	N/C(ALE)
57	FPY:Ground	59	FPY:RDATA	58	N/C(DACK)	60	HD:Ground
61	FPY:Ground	63	FPY:HS	62	HD:IRQ14	64	IOCS16*
65	FPY:Ground	67	FPY:DSCH	66	HD:A1	68	N/C (PDIAG)
69	N/C	71	N/C	70	HD:A0	72	HD:A2
73	N/C	75	N/C	74	HD:CS0*	76	HD:CS1*
77	N/C	79	N/C	78	HD:SLVACT	80	HD:Ground

**Notes:** The following symbols identify to which interface a signal belongs.

**FPY** Floppy Drive Interface (Signal names preceded by “N/C”, for example, N/C (DRQ), indicate that there is currently no connection, but the pins are reserved for future implementation of the indicated signals.)

**HD** EIDE Hard Disk Interface

Table 2– 3. J5 Pinout Summary

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	S1:DCD1	3	S1:DSR1	2	PP:STB*	4	PP:AFD*
5	S1:RXD1	7	S1:RTS1	6	PP:PD0	8	PP:ERR*
9	S1:TXD1	11	S1:CTS1	10	PP:PD1	12	PP:INIT*
13	S1:DTR1	15	S1:RI1	14	PP:PD2	16	PP:SLIN*
17	S1:Ground	19	S1:NC	18	PP:PD3	20	PP:Ground
21	S2:DCD2	23	S2:DSR2	22	PP:PD4	24	PP:Ground
25	S2:RXD2	27	S2:RTS2	26	PP:PD5	28	PP:Ground
29	S2:TXD2	31	S2:CTS2	30	PP:PD6	32	PP:Ground
33	S2:DTR2	35	S2:RI2	34	PP:PD7	36	PP:Ground
37	S2:Ground	39	S2:TXD2-TTL	38	PP:ACK*	40	PP:Ground
41	USBPS0	43	USB:PWR-	42	PP:BSY	44	PP:Ground
45	USB:P0-	47	USB:P0+	46	PP:PE	48	PP:Ground
49	USB:GND	51	USB:PS1-	50	PP:SLCT	52	RXIR2/Mode
53	USB:PWR	55	USB:P1-	54	N/C	56	Ground
57	USB:P1+	59	USB:GND	58	TXIR	60	RXIR
61	MOU:DATA	63	MOU:CLK	62	SPKR+	64	Ground
65	Ground	67	MOU:PWR	66	RESET SW	68	KBD:SW
69	HD:ACTIVE	71	EXTSMI	70	KBD:DATA	72	KBD:CLK
73	NC	75	NC	74	Ground	76	KBD:PWR
77	-12V	79	-5V	78	BATV+	80	BATV-

**Notes:** The following symbols identify to which interface the signal belongs.

**S1** Serial Port 1

**S2** Serial Port 2

**PP** Parallel Port

**KBD** Keyboard

**HD** EIDE Hard Disk

**MOU** PS/2 Mouse Port

**USB** Universal Serial Bus

## Central Processor/Core Logic

The CPU on the CoreModule/P5e is an Intel Pentium with MMX running at 166 MHz or 266 MHz. The board uses the Intel TX chipset to implement the motherboard logic, PCI bus, and PC/104 bus. The board utilizes the on-chip cache of the Pentium CPU chip. There is no secondary cache.

## CPU Thermal and Power Management

The CoreModule/P5e may be equipped with either a passive heatsink or a combination heatsink/fan and also contains a thermal sensor. Together, these serve to extend the module's temperature range to the maximum possible. (Note, however, that the cooling fan may restrict mounting options for the module. The fan must be provided access to adequate air flow. This may require the CoreModule to be the top module in a PC/104 stack. In this case, you can still add expansion cards below the module.)

## Air-Flow Requirements

You must provide adequate air flow to keep the processor within its specified case temperature limit of 95°C. Table 2-4 shows the maximum ambient temperature in which the board can operate, as a function of air flow. As indicated, the airflow requirements differ according to the speed of the CPU and whether the simple heat sink or combination heatsink/fan is being used. The temperatures shown in Table 2-4 assume the CPU is fully active and that power management modes are not activated.

*Table 2-4. Airflow and Maximum Ambient Temperature*

<b>CPU Speed</b>	<b>"Core" Power</b>	<b>Temp Rise Still Air</b>	<b>Temp Rise w/Fan</b>	<b>Speed 200</b>
<b>166 MHz</b>	1.8W	30C	NA	1087 MHz
<b>266 MHz</b>	2.7W	37C	17C	1739 MHz
The standard maximum case temperature for the processor is 95C. The 166MHz processor is available in an extended temperature version.				

## APM Power Management

The CoreModule BIOS provides the option of automatic power management. There are several configuration options, which you can adjust using the BIOS Setup program. These include time delays between activation of power saving states, throttle setting, and selection of events which return the system to its Full On state.

There are four defined power management states: Full On, Doze, Standby, and Suspend. In the Full On state, there is no power management taking place. In other words, the system is running at full speed. In both the Doze and Standby states, a “stop clock” signal is asserted to the CPU (halting its internal operation) for a fraction of the time, from 12.5% to 87.5%. This fraction is called the “Throttle” setting; it is one of the APM configuration parameters that you select using the BIOS Setup program. When the system is in the Full On state, it is at 0% Throttle. When it is in the Suspend state, it is at 100% Throttle; the Suspend state is essentially equivalent to a CPU Halt instruction.

The power savings that result from use of the power management BIOS support is indicated in Table 2-5. The table shows percentages because it is relative to the Full On power, which varies according to whether the CPU clock is configured for 266 MHz or 166 MHz operation. Full On board power at 266 MHz is typically 7.9 w; at 166 MHz, it is 6.1 w.

In the BIOS Setup program, you can select a desired Throttle percentage in eighths, from 87.5% to 12.5%. The result of the Throttle setting is that the CPU is placed in Stop Clock mode for a percentage of its operating time. In other words, if the Throttle setting is 87.5%, then the Stop Clock signal to the CPU is asserted seven eighths of the time. The time delay to transition between APM states (Normal > Doze > Standby > Suspend) is also configured in Setup.

*Table 2-5. CPU “Core Power” vs. APM Settings*

APM State	Throttle Setting (% Stop Clock Assertion)						
	12.5%	25%	37.5%	50%	62.5%	75%	87.5%
<b>Full On</b>	100%	100%	100%	100%	100%	100%	100%
<b>Doze</b>	90%	80%	70%	60%	50%	40%	30%
<b>Standby</b>	90%	80%	70%	60%	50%	40%	30%
<b>Suspend</b>	20%	20%	20%	20%	20%	20%	20%

## Thermal Sensor

A thermal sensor is attached to the board near the Pentium CPU. It senses when the CPU temperature exceeds its upper temperature threshold. Running the CPU at a temperature higher than this threatens a system “crash” or actual damage to the CPU chip and should be avoided. When triggered, the temperature sensor signals the BIOS to reduce CPU clock speed by 50%. In this condition, CPU Core Power reduces by approximately 40%. This speed reduction remains in effect until the processor has reduced its temperature. The

thermal sensor has a 10°C hysteresis, which means that the processor must cool by 10°C, before full speed operation will resume.

## DRAM

The CoreModule/P5e uses an Ampro custom memory module. Versions of the module with 8 MB, 16 MB, 32 MB, and 64 MB are available. (DRAM parity is not implemented.)

**Note:** Memory is installed at the factory; it is not field-upgradable.

When the system boots, the BIOS measures the amount of memory installed and configures the internal memory controller for that amount. No jumpering or manual configuration is required. You can see how much memory the BIOS measured by running Setup.

DRAM memory is allocated as shown in Table 2-6.

Table 2– 6. System Memory Map

Memory Address	Function
FE0000h - FFFFFFFh	Duplicates BIOS at 0E0000-0FFFFFFh.
100000h - FFFFFFFh	Extended memory
0E0000h - 0FFFFFFh	128K ROM BIOS; on-board Flash disk option
0D0000h - 0DFFFFFFh	BIOS extension option, if enabled. Otherwise, free.
0C8000h - 0CFFFFFFh	Available
0C0000h - 0C7FFFh	Video BIOS (when a video controller is installed)
0A0000h - 0BFFFFFFh	Normally contains video RAM, as follows: CGA Video: B8000-BFFFFFFh Monochrome: B0000-B7FFFh EGA and VGA video: A0000-AFFFFFFh
000000h - 09FFFFFFh	Lower 640K DRAM

## On-Board Flash Memory Option

The CoreModule/P5e has an optional on-board NAND Flash memory. It is used for:

- **System BIOS (128K)** — Ampro's enhanced embedded-system BIOS
- **OEM DiskOnChip Drive** — Available for OEM use as a DiskOnChip 2000 drive. The DiskOnChip portion is 8064K bytes.

Special utilities are required to update the BIOS image and to format the DiskOnChip 2000 drive. These utilities are provided on the Utility diskette that comes in the CoreModule/P5e Quickstart Kit (CM3-P5E-K-00) and Literature Set (DOC-CP5-Q-02). See the section in this manual on Utility Software for an explanation on how to use these utilities.

The DiskOnChip 2000 drive can be enabled or disabled in Setup. When enabled, it is treated as a hard drive.

## Interrupt and DMA Channel Usage

The PC architecture provides several interrupt and DMA control signals. When you expand the system through the ISA portion of the PC/104-Plus bus (P1, P2) with MiniModule products or plug-in cards that require either interrupt or DMA support, you must select which interrupt or DMA channel to use. Typically this involves switches or jumpers on the expansion module. In most cases, these are not shared resources. It is important that you configure the new module to use an interrupt or DMA channel not already in use. For your convenience, Table 2-7 and Table 2-8 provide a summary of the normal interrupt and DMA channel assignments on the CoreModule/P5e.

The PCI bus uses four interrupts (INTA\*, INTB\*, INTC\*, and INTD\*). These interrupts are mapped to any of the available ISA interrupts by the BIOS. The PCI bus needs only INTA\* if each PCI device is single function. If an expansion card has multiple functions, then more interrupts may be required. You can set the priority in which interrupts are assigned on Setup 6 — PCI Configuration Setup.

Table 2-7. Interrupt Channel Assignments

Interrupt	Function
IRQ0	ROM BIOS clock tick function, from Timer 0
IRQ1	Keyboard interrupt
IRQ2	Cascade input for IRQ8-15
IRQ3	Serial 2
IRQ4	Serial 1
IRQ5	Available
IRQ6	Floppy controller
IRQ7	Parallel port (option)
IRQ8	Reserved for battery-backed clock alarm
IRQ9	Available
IRQ10	Available
IRQ11	Available
IRQ12	PS/2 Mouse
IRQ13	Reserved for coprocessor
IRQ14	IDE hard disk controller
IRQ15	Available

Table 2–8. DMA Channel Assignments

Channel	Function
0	Available for 8-bit transfers
1	Available for 8-bit transfers (ECP parallel port option)
2	Floppy controller
3	Available for 8-bit transfers (ECP parallel port option)
4	Cascade for channels 0-3
5	Available for 16-bit transfers
6	Available for 16-bit transfers
7	Available for 16-bit transfers

## Watchdog Timer

A unique feature of the on-board clock circuitry is a watchdog timer. You can program this timer to generate an interrupt or reset signal if the programmed time interval expires before the timer is reinitialized. Use Setup to select the time interval and the time-out action during boot. Intervals of 30, 60, and 90 seconds are available.

Unlike previous CoreModules, the Watchdog Timer uses dedicated circuitry instead of the real time clock alarm output.

### Reinitializing, Enabling, and Disabling the Watchdog Timer

The following assembly language code illustrates how to reinitialize, enable, and disable the watchdog timer from within your application program.

```

;-----
; Code to enable or disable the watchdog timer
;-----
MOV  AH,0C3h          ;Watchdog timer BIOS function
MOV  AL,nn           ;Use 00 to disable, 01 to enable
MOV  BX,mm           ;Set mm to the timeout delay, in seconds
                          ;00h - 0FFh = 0 - 255 seconds

INT  15h

```

In order to tickle the watchdog timer, you would need to read I/O port 201h.

# DC Power

## Overview

The CoreModule/P5e CPU requires only +5 volts DC ( $\pm 5\%$ ) for operation. Low voltage for the CPU (~1.9 volts) is supplied by an on-board voltage converter. The same is true for the  $\pm 9$  volts needed for the RS232 serial ports.

You may need to provide +12 volts for an external hard drive or other voltages for other added peripherals.

The board does not support 3.3 volt PCI cards. Only 5 volt or 3.3 volt/5 volt modules configured for 5 volt operation are supported.

The exact power requirement of the CoreModule/P5e CPU system depends on several factors, including CPU speed, the quantity of installed DRAM, any MiniModule products or other expansion boards attached to the PC/104-Plus bus (which draw their power from the PC/104-Plus bus), and any peripherals you have added to your system. For example, AT keyboards draw their power from the board, and there can be some loading from devices connected to the serial and parallel ports.

---

### Note

If you use a switching power supply, be sure it regulates properly with the load your system draws. Some switching power supplies do not regulate properly unless they are loaded to some minimum value. If this is the case with your supply, consult the manufacturer about additional loading, or use another supply or another type of power source (such as a linear supply, batteries, etc.).

---

## Power Connector J7

J7 is the main power connector for the CoreModule/P5e. It is a dual-row 0.100 inch right-angle 10-pin header. Table 2-9 lists the pins on this connector.

*Table 2– 9. Power Connector, J7*

J7 Pin	Signal
2, 8, 10	+5 V
4	+12 V
6	N/C
1, 3, 5, 9	Ground
7	Key

Table 2-10 shows a typical mating connector you can use to attach power to J7.

*Table 2–10. Mating Connector, J7*

<b>Connector</b>	<b>Mating Connector</b>
Discrete Wire, 10-pin	Housing: Berg 69176-010 Pins: Berg 48245-000 Polarizing Plug in position 7: Berg 65307-001

## Backup Battery

You can add an external 3.6 volt lithium battery to power the on-board real-time clock. Connect the positive terminal to J5-78 and the negative terminal to J5-80.

The battery is used only while system power is off. The real-time clock battery drain is approximately 10  $\mu$ A. Here is the formula for calculating battery life (in hours):

$$\text{Battery life} = (\text{mA-hour battery specification} \div (10 \mu\text{A})) \times \text{Duty Cycle}$$

To calculate battery life, divide the battery rating by the clock current. Then, multiply that result by the duty cycle of battery usage. That is, estimate the percentage of time the battery supplies power while the system is off.

# Serial Ports

## Overview

The CoreModule/P5e CPU provides two standard RS232C serial ports. You can use the serial ports for printers, modems, terminals, remote hosts, or other RS232C serial devices. Many serial devices, such as printers and modems, require handshaking in one or both directions. Consult the documentation for the device(s) you use for information about handshaking, cabling, and other interface considerations.

Both serial ports support software selectable baud rates up to 115.2K baud, 5-8 data bits, and 1, 1.5, or 2 stop bits. Note that the IEEE RS232C specification limits the serial port to 19.2K baud on cables up to 50 feet in length.

The serial ports are based on a 16550 UART-compatible controller. This is an advanced UART that has a 16-byte FIFO buffer to improve throughput.

Serial Port 2 can be configured for two additional modes of operation, IrDA or TTL. For information about using the port in IrDA mode, see *Infrared (IrDA) Interface* on page 2-19.

Serial 2's TTL transmit line appears on J5-39. This pin connects directly to the TxD (transmit data) pin of the serial port (without going through the RS232 level converter). Serial 2's RS232 receive line (RxD) can be used for TTL input without needing a different pin. Serial 2's RxD line appears on J5-25.

## I/O Addresses and Interrupts

The serial ports can be configured to appear at any of the standard PC port addresses and interrupts. Each serial port can be independently configured using the Setup function. See *Setup 7 — Integrated Peripherals Setup* on page 2-58 for details about configuring the serial ports.

If you will not be using a serial port in your design, you can disable it, freeing its I/O addresses and interrupt assignments for use by other devices installed on the PC/104-Plus expansion bus.

## ROM-BIOS Installation of the Serial Ports

Normally, the ROM BIOS supports Serial 1 as the DOS COM1 device, Serial 2 as the DOS COM2 device, and so on. If you disable a serial port, and there is no substitute serial port in the system, then the ROM-BIOS assigns the COM designations as it finds the serial ports, starting from the primary serial port and searching to the last one. Thus, for example, if Serial 1 is disabled, the ROM-BIOS assigns COM1 to Serial 2 (unless another Serial 1 is discovered).

The ROM BIOS scans I/O addresses for serial ports in the following order: 3F8h, 2F8h, 3E8h, 2E8h.

## Serial Port Connectors

Both serial ports appear on portions of J5. Their pinouts on J5 are arranged so that a 40-pin ribbon cable attached to J5 can be split to attach two 10-pin DB-9 connectors to match the

PC standard pinout. Table 2-11 gives the connector pinout and signal definitions for both ports.

In addition, the table indicates the pins to which each signal must be wired for compatibility with standard DB25 and DB9 connectors. Normally PC serial ports use male “DB” connectors.

*Table 2– 11. Serial Port Connectors*

<b>J5 Pin</b>	<b>Signal Name</b>	<b>Function</b>	<b>In/Out</b>	<b>DB25 Pin</b>	<b>DB9 Pin</b>
1	DCD1	Data Carrier Detect	In	8	1
3	DSR1	Data Set Ready	In	6	6
5	RXD1	Receive Data	In	3	2
7	RTS1	Request To Send	Out	4	7
9	TXD1	Transmit Data	Out	2	3
11	CTS1	Clear to Send	In	5	8
13	DTR1	Data Terminal Ready	Out	20	4
15	RI1	Ring Indicator	In	22	9
17	GND	Signal Ground	-	7	5
19	NC	-	-	-	-
21	DCD2	Data Carrier Detect	In	8	1
23	DSR2	Data Set Ready	In	6	6
25	RXD2	Receive Data	In	3	2
27	RTS2	Request To Send	Out	4	7
29	TXD2	Transmit Data	Out	2	3
31	CTS2	Clear to Send	In	5	8
33	DTR2	Data Terminal Ready	Out	20	4
35	RI2	Ring Indicator	In	22	9
37	GND	Signal Ground	-	7	5
39	TxD2-TTL	TTL version of TxD2	Out	-	-

## Using a Serial Modem

You can use either of the serial ports to interface to a modem. Generally, you will not need to concern yourself with serial port initialization (baud rate, start bits, stop bits, and so forth) since most retail PC communications programs control the serial port hardware directly. If your program does not do this, use the DOS MODE command to initialize the port.

When installing a modem, be sure to connect appropriate input and output handshake signals, depending on what your communications software requires. Standard PC-compatible serial modem cables that correctly connect all of the proper signals are commonly available.

Many powerful communications programs are available to control modem communications. Some of these programs offer powerful “script” languages that allow you to generate complex automatic applications.

## Serial Console Features

You can connect a device, such as an ASCII video terminal or PC running a video terminal emulation program, to either serial port to act as your system console.

To use the serial console features, connect a serial console device to Serial 1 or Serial 2. Use Setup to enable the serial console feature.

When enabled, the serial console is set up for:

- 9600 baud
- No parity
- 8 bits
- One stop bit

To use an ASCII terminal as the console device for your system, set the serial baud rate, parity, data length, and stop bits of the terminal to match the serial console settings.

For proper display of Setup and POST messages from the BIOS, you must use an IEEE-compatible terminal or terminal emulation program that implements the standard ASCII cursor commands. The required commands and their hexadecimal codes are listed in Table 2-12.

*Table 2–12. Required Cursor Commands*

Hex	Command
08	Backspace
0A	Line Feed
0B	Vertical Tab
0C	Non-destructive Space
0D	Carriage Return

---

**Note:** Some programs that emulate an ASCII terminal do not properly support the basic ASCII command functions shown in Table 2-12. Ampro provides a suitable PC terminal emulator program, TVTERM, on the Common Utilities diskette.

---

After booting this system, the keyboard and screen of the serial terminal become the system console. Note that the programs you execute via the serial terminal must use ROM BIOS video functions (rather than direct screen addressing) for their display I/O.

**Note**

---

DOS programs that write directly to video RAM will not display properly on a serial console device.

---

### *Using a Standard PC Keyboard*

If you have both a serial terminal and a standard keyboard attached to your system at the same time, both keyboards will function.

### *Using Arrow Keys During Setup*

During Setup, the serial console arrow keys and function keys must be simulated.

The **arrow keys** are simulated with the substitute keystrokes shown in Table 2-13:

*Table 2– 13. Arrow Key Substitutions*

<b>Function</b>	<b>Substitute Keys</b>
Up	^ or Ctrl e
Down	v or Ctrl x
Right	> or Ctrl d
Left	< or Ctrl s
PgUp	Ctrl r
PgDn	Ctrl c

The **function keys** are simulated by entering two keystrokes, an “F” followed by the function key number. Thus, function key F3 is simulated with the literal “F3” typed on the keyboard. (Don’t type the quotes). F10 is simulated with “F0”.

Note that these keystroke simulations are only valid during Setup, not during normal operation.

### *COM Port Table*

When the system boots under DOS, the serial ports are initialized to 9600 baud (typical). To preserve the selected console port parameters stored in Setup, the Ampro ROM BIOS deletes the selected console port from the internal COM port table, normally used by DOS to locate the serial ports. With the port deleted from the COM port table, DOS cannot change its parameters. Because it is not listed in the BIOS COM port table, it is not assigned a COMn designation (COM1, COM2, etc.).

## Serial Booting and Serial Downloading

Serial console functionality has been expanded to incorporate two additional features useful in embedded applications.

- The *serial boot* facility enables the CoreModule/P5e to boot from code downloaded through a serial port in a manner similar to booting from a local hard disk or from a network.
- The *serial downloading* facility permits updating the software installed in the on-board Disk-On-Chip 2000 drive over the serial port.

Refer to Ampro Application Note AAN-9403 for a complete description of these features. Refer to the Ampro Common Utilities manual for descriptions of the utility programs used to support serial booting and serial downloading.

## Infrared (IrDA) Interface

The CoreModule/P5e infrared interface provides for a two-way wireless communications port using infrared as a transmission medium. The CoreModule/P5e IrDA interface supports both SIR (Serial Infrared) and FIR (Fast Infrared) standards. The SIR standard allows serial communication at baud rates up to 115K Baud. The FIR standard allows data rates up to 4 Mbits/second.

### Requirements for an IrDA interface

On the CoreModule/P5e, the IrDA physical link hardware consists of an IR transmit encoder and IR receiver decoder. To implement an IrDA port, the OEM must supply an IR transducer, which consists of the output driver and IR emitter for transmitting, and the receiver IR detector. Particular IR transducers may require additional external components.

The IrDA port uses the second serial port to drive its internal encoder/decoder. When using the IrDA interface, you cannot use serial 2 as an RS232 port.

The IrDA interface encodes its output such that "0" is represented by a pulse and "1" is represented by no pulse. A pulse occupies a minimum of 1.6 microseconds to a maximum of 3/16th of a bit period, depending on the bit rate of the data. This pulse stream forms the input to the driver for the IR emitter that converts the electrical pulses to IR energy.

The IrDA port pinout is listed in Table 2-14.

*Table 2-14. IrDA Interface Pinout*

<b>J5 Pin</b>	<b>Signal Name</b>	<b>Function</b>
52	FIR/M	Fast IR Receive/Mode Output:
56	GND	Signal Ground
58	TxIR	IR Transmit
60	RxIR	IR Receive (SIR)

There are two popular implementations of Fast IR. One uses a separate receive line capable of receiving at the higher data rate (up to 4 Mbytes/second). The other is implemented with a mode control line. When the IR port is set for high speed, the mode output line (FIR/M, J5-52) is high. This switches the external transceiver to high speed mode.

# Parallel Port

## Overview

The enhanced parallel printer port is a superset of the standard PC-compatible printer port. It supports four modes of operation:

- **Standard PC/AT printer port** — Centronics-type output only printer port, compatible with the original IBM PC printer port.
- **Bi-directional parallel port** — Sometimes called a PS/2-compatible parallel port. As an output, it behaves the same as the standard PC/AT port, and provides an input mode as well.
- **Enhanced Parallel Port (EPP)** — Bi-directional parallel port, compatible with the Standard and PS/2 ports. Adds automatic read- and write-cycle modes. Automatically generates input and output handshaking signals for increased throughput. Data flow is monitored by a parallel port watchdog timer (separate from the board's watchdog timer) to ensure reliable transfers.
- **Extended Capabilities Parallel Port (ECP)** — Compliant with the IEEE-1284 Extended Capabilities Port Protocol and ISA Standard (Rev 1.09, January 7, 1993), developed by Microsoft. The ECP mode provides the highest level throughput for the parallel port. It provides interlocking handshaking, a 16-byte FIFO buffer, DMA transfers (optional), hardware RLE data compression (optional), and well-defined software protocols.

## I/O Addresses and Interrupts

The parallel port functions are controlled by eight I/O ports and their associated register and control functionality. The CoreModule/P5e parallel port is assigned to the primary parallel port address normally assigned to LPT1 and cannot be changed. You may disable the port in Setup to free the hardware resources for other peripherals.

The parallel port can be configured to generate an interrupt request upon a variety of conditions, depending on the mode the port is in. Assignment of an interrupt to the parallel port is optional, and its use depends on software requirements and which mode of operation you are using. IRQ 7 is assigned to the parallel port.

Table 2-15 lists the parallel port addresses and interrupt request..

*Table 2–15. Parallel Printer I/O Addresses and Interrupt*

<b>Selection</b>	<b>I/O Address</b>	<b>Interrupt</b>
Primary	378h - 37Fh	7
Secondary	278h - 27Fh	5
Secondary	3BCh - 3BFh	None
Disable	None	None

### *ROM-BIOS Installation of Parallel Ports*

Normally, the BIOS assigns the name LPT1 to the primary parallel port, and LPT2 to the secondary parallel port (if present), and so on. However, the BIOS scans the standard addresses for parallel ports and if it only finds a secondary port, it assigns LPT1 to that one. Therefore, if the CoreModule's parallel port is enabled, it will be assigned LPT1 by the BIOS. If it is disabled and there is another parallel port in your system, that port will be assigned LPT1 by the BIOS.

The ROM-BIOS scans I/O addresses for parallel ports in the following order: 3BCh, 378h, 278h.

## DMA Channels

In ECP enhancement mode, the parallel port can send and receive data under control of an on-board DMA controller. DMA channels operate with a request/acknowledge hardware handshake protocol between an internal DMA controller and the parallel port logic. On the CoreModule/P5e, select a DMA channel in Setup. You can configure the parallel port to use either DMA channel 1 or DMA channel 3.

If you will not be using DMA with the parallel port, leave it disabled. This makes the DMA channel available to other peripherals installed on the expansion buses.

## Parallel Port Connector

The parallel port appears on a portion of J5. Its pinout on J5 is arranged so that a 40-pin ribbon cable attached to J5 can be split to attach a 25-pin DB-25 connector to match the PC standard. Table 2-16 gives the connector pinout and signal definitions for the parallel port.

In addition, the table indicates the pins to which each signal must be wired for compatibility with a standard DB25 connector. Normally the PC parallel port uses a female “DB” connector.

*Table 2–16. Parallel Port Connections (J5)*

<b>J5 Pin</b>	<b>Signal Name</b>	<b>Function</b>	<b>In/Out</b>	<b>DB25 Pin</b>
2	STB*	Output Data Strobe	Out	1
6	PD 0	LSB Of Printer Data	I/O	2
10	PD 1		I/O	3
14	PD 2		I/O	4
18	PD 3		I/O	5
22	PD 4		I/O	6
26	PD 5		I/O	7
30	PD 6		I/O	8
34	PD 7	MSB Of Printer Data	I/O	9
38	ACK*	Character Accepted	In	10
42	BUSY	Cannot Receive Data	In	11
46	PE	Out of Paper	In	12
50	SLCT	Printer Selected	In	13
4	AUTOFD*	Autofeed	Out	14
8	ERROR	Printer Error	In	15
12	INIT*	Initialize Printer	Out	16
16	SELIN*	Selects Printer	Out	17
20, 24, 28, 32, 36, 40, 44, 48	GND	Signal Ground	N/A	18 - 25

### Note

---

For maximum reliability, keep the cable between the board and the device it drives to 10 feet or less in length.

---

Table 2-17 lists the signal specifications for the parallel port signals.

*Table 2– 17. Parallel Port Signal Specifications*

<b>Signal</b>	<b>Signal Specification</b>
PD0 - PD7	24mA Sink 12mA Source
ERROR* SLCT PE ACK* BUSY	TTL Input
STB* AUTOFD* INIT* SELIN*	24 mA Sink 4.7k Pull up

### *IEEE-1284-compliant Cables*

Using the parallel port for high-speed data transfer in ECP/EPP modes requires special cabling for maximum reliability.

Some of the parameters for a compliant IEEE-1284 cable assembly include:

- All signals are twisted pair with a signal and ground return
- Each signal and ground return should have a characteristic unbalanced impedance of 62 +/- 6 ohms within a frequency band of 4 to 16 MHz
- The wire-to-wire crosstalk should be no greater than 10%

Please refer to the IEEE-1284 standard for the complete list of requirements for a compliant cable assembly, including recommended connectors

### *Latch Up Protection*

The parallel port incorporates chip protection circuitry on some inputs, designed to minimize the possibility of CMOS “latch up” due to a printer or other peripheral being powered up while the CoreModule/P5e is turned off.

## **Parallel Port Registers**

The low-level software interface to the parallel port consists of eight addressable registers. The address map of these registers is shown in Table 2-18.

Table 2– 18. Parallel Port Register Map

Register Name	Address
Data Port	Base address
Status Port	Base address + 1
Control Port	Base address + 2
EPP Address Port	Base address + 3
EPP Data Port 0	Base address + 4
EPP Data Port 1	Base address + 5
EPP Data Port 2	Base address + 6
EPP Data Port 3	Base address + 7
<b>Note:</b> EPP registers are only accessible when in EPP mode	

## Standard and Bi-Directional Operation

You can use the parallel port as a standard output-only printer port or as a PS/2-compatible bi-directional data port with up to 12 output lines and 17 input lines. The bi-directional mode can be very valuable in custom applications. For example, you might use it to control an LCD display, scan keyboards, sense switches, or interface with optically isolated I/O modules. All data and interface control signals are TTL-compatible.

Set the parallel port's default mode using Setup.

### *Using the Parallel Port in Bi-Directional Mode*

To use the port as a bi-directional data or digital control port you must set the default mode to bi-directional in Setup or put it in bi-directional mode with a BIOS call. The following code example shows how to set the parallel port mode to bi-directional.

```

;-----
; Code to set the parallel port mode to bi-directional
;-----
MOV  AH,0CDh          ; AMPRO command
MOV  AL,0Ch           ; AMPRO function
MOV  BX,01h           ; Extended mode (use 00 to set output-only mode)
INT  13h

```

Within bi-directional mode, the port can be in its input state or output state. The code shown above leaves the port in its input state. An IN instruction of I/O address 378h reads the current state of the data lines.

To change the port between input and output states, write a 1 to bit five of the control register to set the port to its input state; or a 0 to set it to its output state. Here is a code sample for dynamically changing the port direction (after it is in Extended Mode).

```

;-----
; Code to change the parallel port direction to input
;-----
MOV    DX,37A
IN AL,DX
OR AL,20h           ;set bit 5 (input)
OUT    DX,AL
;
;-----
; Code to change the parallel port direction to output
;-----
MOV    DX,37Ah
IN AL,DX
AND    AL,0DFh      ;clear bit 5
OUT    DX,AL

```

### *Using the Control Lines for Additional I/O*

Besides the eight data lines, you can use the four control lines (STB\*, AUTOFD\*, INIT\*, and SELIN\*) as general purpose output lines. Similarly, you can use the five status lines (ERROR\*, SLCT, PE, ACK\*, and BUSY) as general purpose input lines.

You can read the four control lines and use them as input lines. These lines have open collector drivers with 4.7K ohm pull-ups. To use a control line as an input line, you must first write to its corresponding bit in the control register. If the line is inverting (\*), write a 0, otherwise write a 1. This will cause the line to float (pulled up by the 4.7K ohm resistors). When a line floats, you can use it as an input.

### *Enabling the Parallel Port Interrupt*

Bit 4 in the Control Register enables the parallel port interrupt. If this bit is high 1, then a rising edge on the ACK\* (IRQ) line will produce an interrupt on the parallel port interrupt, IRQ7.

Table 2-19 lists the parallel port register bits.

Table 2-19. Parallel Port Register Bits

Register	Bit	Signal Name or Function	In/Out	Active High/Low	J5 Pin	DB25F Pin
DATA (378h)	0	PD 0	I/O	High	6	2
	1	PD 1	I/O	High	10	3
	2	PD 2	I/O	High	14	4
	3	PD 3	I/O	High	18	5
	4	PD 4	I/O	High	22	6
	5	PD 5	I/O	High	26	7
	6	PD 6	I/O	High	30	8
	7	PD 7	I/O	High	34	9
STATUS (379h)	0	TMOUT	In	---	---	---
	1	0	---	---	---	---
	2	0	---	---	---	---
	3	ERROR*	In	Low	8	15
	4	SLCT	In	High	50	13
	5	PE	In	High	46	12
	6	ACK* (IRQ)	In	Low	38	10
	7	BUSY	In	High	42	11
CONTROL (37Ah)	0	STB*	Out*	Low	2	1
	1	AUTOFD*	Out*	Low	4	14
	2	INIT*	Out*	High	12	16
	3	SELIN*	Out*	High	16	17
	4	IRQE	---	High	---	---
	5	PCD	---	High	---	---
	6	1	---	---	---	---
	7	1	---	---	---	---
* Can also be used as input (see text).						

Parallel port register bit definitions (Table 2-20):

Table 2– 20. Standard and EPP Mode Register Bit Definitions

Signal Name	Full Name	Description
TMOUT	Time-out	Valid only in EPP mode , this signal goes true after a 10 $\mu$ S time-out has occurred on the EPP bus. This bit is cleared by reset.
ERR*	Error	Reflects the status of the -ERROR input. 0 means an error has occurred.
SLCT	Printer selected status	Reflects the status of the SLCT input. 1 means a printer is on-line.
PE	Paper end	Reflects the status of the PE input. 1 indicates paper end.
ACK*	Acknowledge	Reflects the status of the ACK input. 0 indicates a printer received a character..
BUSY*	Busy	Reflects the complement of the BUSY input. 0 indicates a printer is busy.
STB*	Strobe	This bit is inverted and output to the - STROBE pin.
AUTOFD	Auto feed	This bit is inverted and output to the - AUTOFD pin.
INIT*	Initiate output	This bit is output to the -INIT pin.
SELIN*	Printer select input	This bit is inverted and output to the pin. It selects a printer.
IRQE	Interrupt request enable	When set to 1, interrupts are enabled. An interrupt is generated by the positive-going - ACK input.
PCD	Parallel control direction	When set to 1, port is in input mode. In printer mode, the printer is always in output mode regardless of the state of this bit.
PD0-PD7	Parallel Data Bits	

## **EPP and ECP Operation**

The board's parallel port is compliant with the IEEE-1284 Extended Capabilities Port Protocol and ISA Standard (Rev 1.09, January 7, 1993), developed by Microsoft. Contact IEEE Customer Service and request IEEE Std 1284 for information about EPP and ECP operation.

IEEE Customer Service  
445 Hoes Lane  
PO Box 1331  
Piscataway, NJ 08855-1331 USA

Phone: (800) 678-IEEE (in the US and Canada)  
(908) 981-0060 (outside the US and Canada)

FAX: (908) 981-9667

Telex: 833233

Website: <http://standards.IEEE.org>

## Floppy Drive Interface

The on-board floppy disk controller and ROM BIOS support one or two floppy disk drives in any of the standard PC formats, from 360K to 1.44M. It has an enhanced digital data separator supporting from 250 Kbps up to 2 Mbps. In addition to floppy drives, it is also capable of interfacing many standard tape drives designed to connect to the floppy drive interface.

### Floppy Drive Considerations

Nearly any type of soft-sectored, single or double-sided, 40 or 80 track, 5-1/4 inch or 3-1/2 inch floppy disk drive is usable with this interface. Using higher quality drives improves system reliability. Here are some considerations about the selection, configuration, and connection of floppy drives to the CoreModule/P5e.

- **Drive Interface** — The drives must be compatible with the board's floppy disk connector signal interface, as described below. Ampro recommends any standard PC-or AT-compatible 5-1/4 inch or 3-1/2 inch floppy drive.
- **Drive Quality** — Use high quality, DC servo, direct drive motor floppy disk drives.
- **Drive Select Jumpering** — Both drives must be jumpered to the second drive select.
- **Floppy Cable** — For systems with two drives, use a floppy cable with conductors 10-16 twisted between the two drives. This is standard practice for PC-compatible systems.
- **Drive Termination** — Resistive terminations should be installed only on the drive connected to the last interface cable connector (farthest from the board). Near-end cable termination is provided on the CoreModule/P5e.
- **Head Load Jumpering** — When using drives with a Head Load option, jumper the drive for head load with motor on rather than head load with drive select. This is the default for PC-compatible drives.
- **Drive Mounting** — If you mount a floppy drive very close to the CoreModule or another source of EMI, you may need to place a thin metal shield between the disk drive and the device to reduce the possibility of electromagnetic interference.

### Floppy Interface Configuration

The floppy interface is configured using Setup to set the number and type of floppy drives connected to the system. Refer to the Setup section on page 49 for details.

If you don't use the floppy interface, disable it in Setup. This frees the floppy's I/O addresses, IRQ6, and DMA channel 2 for use by other peripherals installed on the PC/104 bus.

### Floppy Interface Connector

Table 2-21 shows the pinout and signal definitions of the floppy disk interface which can be found on connector, J4. The pinout of this segment of J4 meets the AT standard for floppy drive cables. The pinout is arranged so that a 40-pin ribbon cable can be split to attach a standard 34-pin floppy drive connector.

Table 2– 21. Floppy Disk Interface Connector

J4 Pin	Fpy Cable	Signal Name	Function	In/Out
3	2	DEN	Speed/Precomp	Out
7	4		N/C	N/A
11	6	Key	N/C	N/A
15	8	IDX*	Index Pulse	In
19	10	MO0*	Motor On 0	Out
23	12	DS1*	Drive Select 1	Out
27	14	DS0*	Drive Select 0	Out
31	16	MO1*	Motor On 1	Out
35	18	DIR*	Direction Select	Out
39	20	STEP*	Step	Out
43	22	WD*	Write Data	Out
47	24	WE*	Write Enable	Out
51	26	TRKO*	Track 0	In
55	28	WP*	Write Protect	In
59	30	RDD*	Read Data	In
63	32	HS*	Head Select	Out
67	34	DCHG*	Disk Change	In
1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61, 65	(all odd) 1 - 33	Ground	Signal grounds	N/a

## EIDE Hard Disk Drive Interface

The CoreModule/P5e provides an interface for one or two Integrated Device Electronics (IDE) peripheral devices, such as hard disk drives and CD-ROM drives.

The EIDE disk controller is an extended IDE interface. It provides features to support large IDE disk drives, logical block addressing (LBA), and supports the Ultra DMA/33 synchronous DMA transfer mode. The Ultra DMA/33 mode provides data throughput of up to 33 MB/S.

A standard IDE interface appears at a portion of connector J4. Its pinout on J4 is arranged so that the ribbon cable can run directly to a 40-pin IDE drive cable connector. EIDE interface signals and pin outs for connector J4 are shown in Table 2-22.

---

### Note

For maximum reliability, keep IDE drive cables less than 18 inches long.

---

Table 2– 22. IDE Interface Connector

J4 Pin	IDE Pin	Signal Name	Function	In/Out
2	1	HOST RESET*	Reset signal from host	OUT
6	3	HOST D7	Data bit 7	I/O
8	4	HOST D8	Data bit 8	I/O
10	5	HOST D6	Data bit 6	I/O
12	6	HOST D9	Data bit 9	I/O
14	7	HOST D5	Data bit 5	I/O
16	8	HOST D10	Data bit 10	I/O
18	9	HOST D4	Data bit 4	I/O
20	10	HOST D11	Data bit 11	I/O
22	11	HOST D3	Data bit 3	I/O
24	12	HOST D12	Data bit 12	I/O
26	13	HOST D2	Data bit 2	I/O
28	14	HOST D13	Data bit 13	I/O
30	15	HOST D1	Data bit 1	I/O
32	16	HOST D14	Data bit 14	I/O
34	17	HOST D0	Data bit 0	I/O
36	18	HOST D15	Data bit 15	I/O
40	20	KEY	Key pin	N/C
42	21	NC (DRQ)	DMA Request	OUT
46	23	HOST IOW*	Write strobe	OUT
50	25	HOST IOR*	Read strobe	OUT
54	27	IDERDY	I/O Channel Ready	OUT
56	28	NC (IDEALE)	Address Latch Enable	10K PU
58	29	NC (DACK)	DMA Acknowledge	IN
62	31	HOST IRQ14	Drive interrupt request	IN
64	32	IDE16	IOCS16	1K PU
66	33	HOST A1	Drive address 1	OUT
68	34	NC (PDIAG)	N/C	N/C
70	35	HOST A0	Drive address 0	OUT
72	36	HOST A2	Drive address 2	OUT
74	37	HOST CS0*	Chip select	OUT
76	38	HOST CS1*	Chip select	OUT
78	39	SLVACT	SLVACT	1K PU
4,38,44, 48, 52, 60, 80	2, 19, 22, 24, 26, 30, 40	GND	Ground	N/A

## IDE Interface Configuration

Use Setup to specify your IDE hard disk drive types. Refer to *Setup 2 — Standard CMOS Setup* on page 2-48 for details.

All IDE drives can report their setup information when queried by the BIOS. Use drive type AUTO to configure the system for IDE drives.

If autoconfigure does not work for your drives, because they were originally misconfigured, you can manually enter drive parameters previously used (or supplied by the drive manufacturer). Use drive type USER to manually enter the drive's parameters

## Universal Serial Bus (USB) Ports

The Universal Serial Bus connects USB devices with a USB host, in this case, the CoreModule/P5e. The USB physical interconnect is a tiered star topology, or tree, consisting of hubs and USB devices. Each USB segment is a point-to-point connection between hubs or between hubs and USB devices. The entire tree can support up to 127 USB devices. This new interface standard is intended for keyboards, mice, modems, digitizer pads, and other low to medium speed peripherals.

Each USB interface is implemented as a two-wire differential pair for data, a power wire, a power sense wire, and a ground wire. The USB port signals appear on J5 as shown in Table 2-23.

Table 2– 23. USB Port Pinout

J5 Pin	Signal Name	Function
41	USB1 PS	USB1 Power Sense
43	USB1 PWR	USB1 +5 Volt Power
45	USB1 D-	USB1 Data-
47	USB1 D+	USB1 Data+
49	Gnd	Ground
51	USB2 PS	USB2 Power Sense
53	USB2 PWR	USB2 +5 Volt Power
55	USB2 D-	USB2 Data-
57	USB2 D+	USB2 Data+
59	Gnd	Ground

The bus can run at 12 Mbits/second or 1.5 Mbits/second, depending on a pull-up on the peripheral device. A 1.5 KOhm pull-up on the +data line sets the speed to 12 Mbits/second. A 1.5 KOhm pull-up on the -data line sets the speed to 1.5 Mbits/second.

The power to the peripheral device must be current limited with a fuse, circuit breaker, or similar device. There is a power-sense input at the host to detect a loss of power.

The CoreModule/P5e has two USB ports. Additional support circuitry, consisting of fuse device, EMI filtering, power-sense resistor divider, and USB connectors, must be provided off-board to implement the ports.

Figure 2- 2 shows a typical USB implementation, including fuse, power supply sense resistor divider, EMI filtering, and USB connector. The 10-Pin connector in this circuit is designed to accept a 10 position cable with the pin-out shown in Table 2-23. Table 2-24 has typical values for the USB circuit, including a vendor list. Entries on this list do not imply

recommendation by Ampro, and are not exhaustive. An assembly based on this design is available from Ampro.

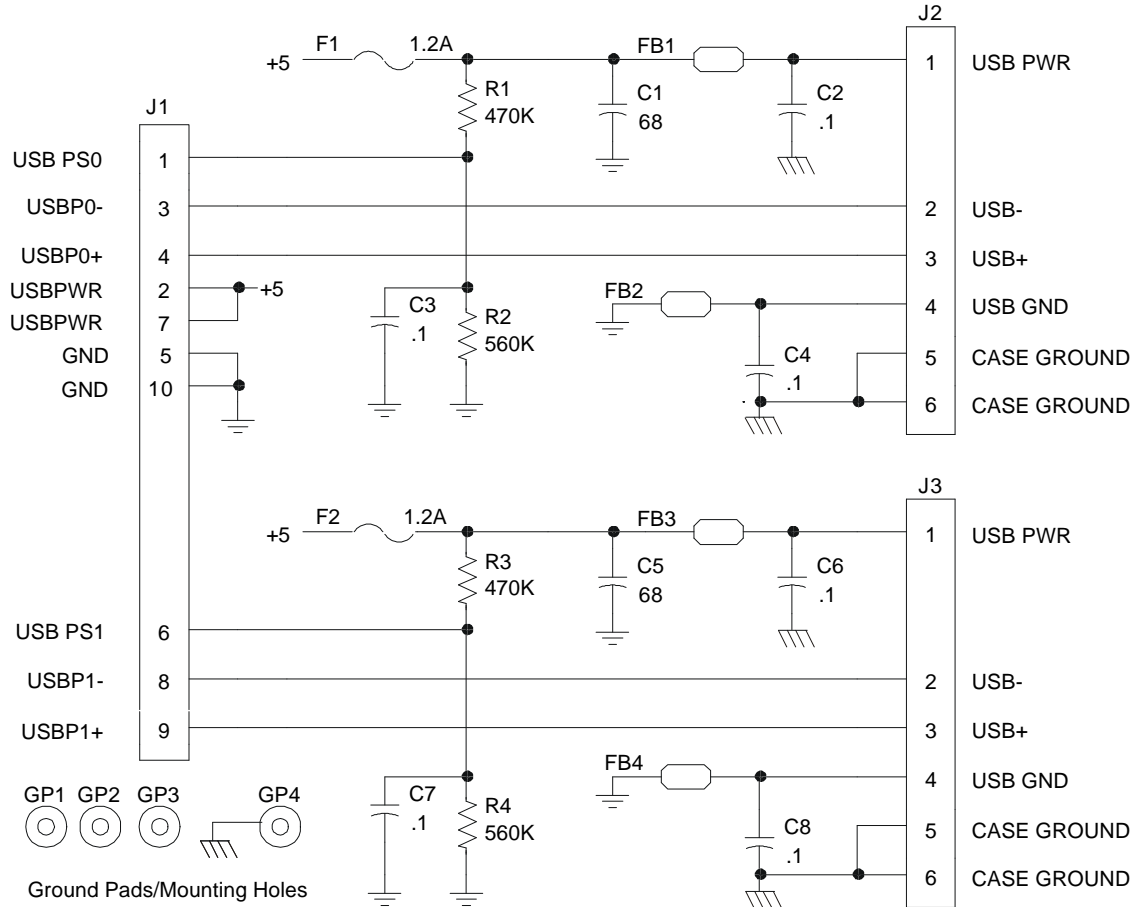


Figure 2–2. Typical USB Interface

Table 2- 24. USB Components

COMPONENT	MANUFACTURER	PART NUMBER
CAP, CER, RAD, .1UF, 20%, 50V	SPRAGUE	1C20Z5U104M050B
CAP, TANT, 68UF, 10V, 20%, RADIAL, DIPPED	KEMET	T353H686M010AS
	NEMCO	PDT68/10ME2
CONN, USB 'A' RECEPTACLE, PCB MOUNT	AMP	787761-1
	BERG	87520-0010A
	BERG	87520-0010B
HDR, 10 POS, DR, GOLD	CIRCUIT ASSEMBLY	CA-D10-23B-43
	MOLEX	10-89-1101
	ASTRON	AT-PH11-10-2-0-GF
INDUCTOR, FERRITE BEAD, AXIAL LEAD	MURATA	BL01RN1-A62
	FAIR-RITE	2773015112
RES, CF, 470K OHM, 1/4W, 5%	KOA	CF1/4-474-J-T52
	ROHM	R25XT68J474
RES, CF, 560K OHM, 1/4W, 5%	KOA	CF1/4-564-J-T52
	ROHM	R25XT68J564
RES, PTC THERMISTOR, 1.2A	BOURNS	MF-R075-2

## PC/104-Plus Expansion Bus

The PC/104-Plus expansion bus appears on three stackthrough header connectors, P1, P2, and P3. P1 is a 64-pin dual-row header. P2 is a 40-pin dual-row header, and P3 is a 120-pin 2mm quad-row header (4 x 30). The PC-bus subset of the PC/104-Plus expansion bus connects to P1. The AT expansion bus signals connect to P2. The layout of signals on P1 and P2 is compliant with the PC/104 bus specification, and make up the ISA bus portion of the PC/104-Plus bus. An implementation of the PCI bus appears on P3.

PC/104-compatible expansion modules can be installed on the CoreModule/P5e expansion bus. The buffered output signals to the expansion bus are standard TTL level signals. All inputs to the CoreModule/P5e operate at TTL levels and present a typical CMOS load to the expansion bus. The current ratings for the output signals driving PC/104-Plus bus are compliant with the PC/104-Plus specification.

## On-board MiniModule Expansion

You can install one or more Ampro MiniModule products or other PC/104 modules on the CoreModule/P5e expansion connectors. When installed on P1 and P2, the expansion modules fit within the CoreModule/P5e's outline dimensions. Most Ampro MiniModule products have stackthrough connectors compatible with the PC/104 specification. You can stack several modules on the CoreModule/P5e headers. Each additional module increases the thickness of the package by 0.66 inches (15 mm). See Figure 2- 3.

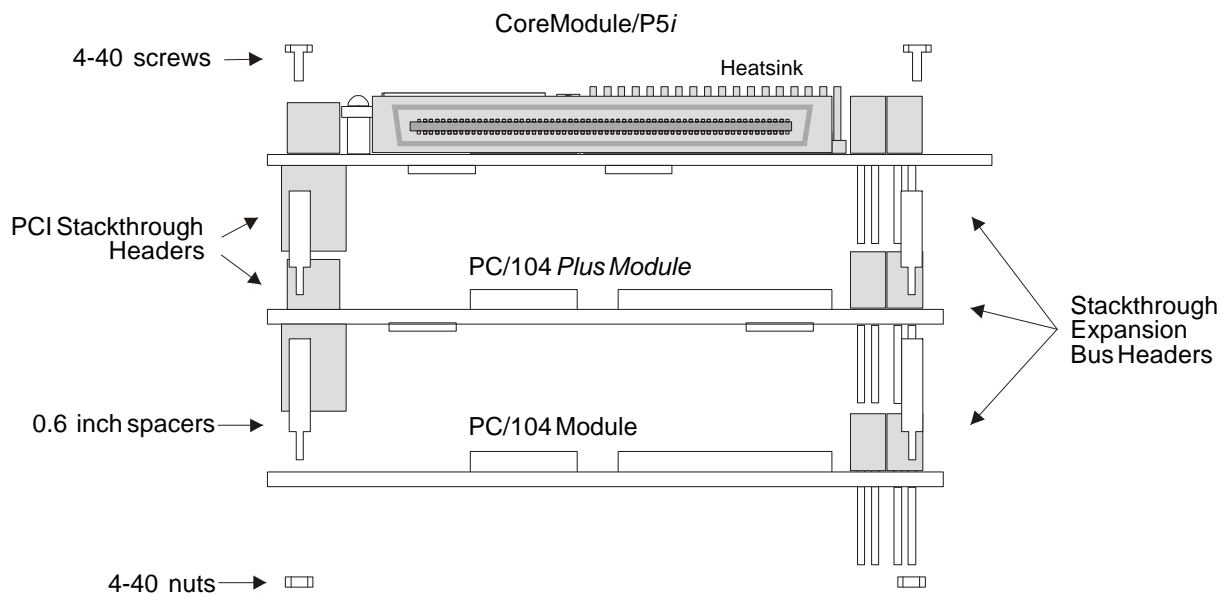


Figure 2- 3. Stacking PC/104-Plus and PC/104 Modules on the CoreModule/P5e

## Using Standard ISA Bus Cards

Ampro offers a development platform that allow you to add conventional 8-bit and 16-bit ISA expansion cards and PCI expansion cards to a CoreModule/P5e system. Contact Ampro for further information about optional bus expansion products.

## Expansion Bus Connector Pinouts

Table 2-25 through Table 2-29 show the pinout and signal functions on the PC/104-*Plus*-compatible expansion bus connectors. These include P1, P2, and P3.

The CoreModule/P5e does not generate  $\pm 12\text{VDC}$  or  $-5\text{VDC}$  for the expansion bus. If devices on the bus require these voltages,  $-12\text{V}$  and  $-5\text{V}$  can be supplied to the bus connector from the PC/104 bus or J5.  $+12\text{V}$  can be supplied through the power connector J7. If a PCI peripheral board requires  $3.3\text{V}$ , you can also attach this voltage to the power connector, J7.

The expansion bus pin numbers for P1 and P2, shown in the following tables, correspond to the scheme normally used on ISA expansion bus card sockets. Rather than numerical designations (1, 2, 3) they have alpha-numeric designations (A1, A2..., B1, B2..., etc.). Similarly, the rows of P3 are designated A, B, C, and D.

Table 2– 25. PC/104 Expansion Bus Connector, P1 (A1-A32)

<b>Pin</b>	<b>Signal Name</b>	<b>Function</b>	<b>In/Out</b>
A1	IOCHCK*	Bus NMI input	IN
A2	SD7	Data bit 7	I/O
A3	SD6	Data bit 6	I/O
A4	SD5	Data bit 5	I/O
A5	SD4	Data bit 4	I/O
A6	SD3	Data bit 3	I/O
A7	SD2	Data bit 2	I/O
A8	SD1	Data bit 1	I/O
A9	SD0	Data bit 0	I/O
A10	IOCHRDY	Processor Ready Ctrl	IN
A11	AEN	Address Enable	I/O
A12	SA19	Address bit 19	I/O
A13	SA18	Address bit 18	I/O
A14	SA17	Address bit 17	I/O
A15	SA16	Address bit 16	I/O
A16	SA15	Address bit 15	I/O
A17	SA14	Address bit 14	I/O
A18	SA13	Address bit 13	I/O
A19	SA12	Address bit 12	I/O
A20	SA11	Address bit 11	I/O
A21	SA10	Address bit 10	I/O
A22	SA9	Address bit 9	I/O
A23	SA8	Address bit 8	I/O
A24	SA7	Address bit 7	I/O
A25	SA6	Address bit 6	I/O
A26	SA5	Address bit 5	I/O
A27	SA4	Address bit 4	I/O
A28	SA3	Address bit 3	I/O
A29	SA2	Address bit 2	I/O
A30	SA1	Address bit 1	I/O
A31	SA0	Address bit 0	I/O
A32	GND	Ground	N/A

Table 2– 26. PC/104 Expansion Bus Connector, P1 (B1-B32)

Pin	Signal Name	Function	In/Out
B1	GND	Ground	N/A
B2	RESETDRV	System reset signal	OUT
B3	+5V	+5 Volt power	N/A
B4	IRQ9	Interrupt request 9	IN
B5	-5V	To J16-3	N/A
B6	DRQ2	DMA request 2	IN
B7	-12V	To J16-1	N/A
B8	ENDXFR*	Zero wait state	IN
B9	+12V	To J10-1	N/A
B10	N/A	Keyed pin	N/A
B11	SMEMW*	Mem Write(lwr 1MB)	I/O
B12	SMEMR*	Mem Read(lwr 1MB)	I/O
B13	IOW	I/O Write	I/O
B14	IOR	I/O Read	I/O
B15	DACK3*	DMA Acknowledge 3	OUT
B16	DRQ3	DMA Request 3	IN
B17	DACK1*	DMA Acknowledge 1	OUT
B18	DRQ1	DMA Request 1	IN
B19	REFRESH*	Memory Refresh	I/O
B20	SYSCLK	Sys Clock	OUT
B21	IRQ7	Interrupt Request 7	IN
B22	IRQ6	Interrupt Request 6	IN
B23	IRQ5	Interrupt Request 5	IN
B24	IRQ4	Interrupt Request 4	IN
B25	IRQ3	Interrupt Request 3	IN
B26	DACK2*	DMA Acknowledge 2	OUT
B27	TC	DMA Terminal Count	OUT
B28	BALE	Address latch enable	OUT
B29	+5V	+5V power	N/A
B30	OSC	14.3 MHz clock	OUT
B31	GND	Ground	N/A
B32	GND	Ground	N/A

Table 2– 27. PC/104 Expansion Bus Connector, P2 (C0-C19)

<b>Pin</b>	<b>Signal Name</b>	<b>Function</b>	<b>In/Out</b>
C0	GND	Ground	N/A
C1	SBHE	Bus High Enable	I/O
C2	LA23	Address bit 23	I/O
C3	LA22	Address bit 22	I/O
C4	LA21	Address bit 21	I/O
C5	LA20	Address bit 20	I/O
C6	LA19	Address bit 19	I/O
C7	LA18	Address bit 18	I/O
C8	LA17	Address bit 17	I/O
C9	MEMR*	Memory Read	I/O
C10	MEMW*	Memory Write	I/O
C11	SD8	Data Bit 8	I/O
C12	SD9	Data Bit 9	I/O
C13	SD10	Data Bit 10	I/O
C14	SD11	Data Bit 11	I/O
C15	SD12	Data Bit 12	I/O
C16	SD13	Data Bit 13	I/O
C17	SD14	Data Bit 14	I/O
C18	SD15	Data Bit 15	I/O
C19	Key	Key Pin	N/A

Table 2– 28. PC/104 Expansion Bus Connector, P2 (D0-D19)

<b>Pin</b>	<b>Signal Name</b>	<b>Function</b>	<b>In/Out</b>
D0	GND	Ground	N/A
D1	MEMCS16*	16-bit Mem Access	IN
D2	IOCS16*	16-bit I/O Access	IN
D3	IRQ10	Interrupt Request 10	IN
D4	IRQ11	Interrupt Request 11	IN
D5	IRQ12	Interrupt Request 12	IN
D6	IRQ15	Interrupt Request 15	IN
D7	IRQ14	Interrupt Request 14	IN
D8	DACK0*	DMA Acknowledge 0	OUT
D9	DRQ0	DMA Request 0	IN
D10	DACK5*	DMA Acknowledge 5	OUT
D11	DRQ5	DMA Request 5	IN
D12	DACK6*	DMA Acknowledge 6	OUT
D13	DRQ6	DMA Request 6	IN
D14	DACK7*	DMA Acknowledge 7	OUT
D15	DRQ7	DMA Request 7	IN
D16	+5V	+5 Volt Power	N/A
D17	MASTER*	Bus Master Assert	IN
D18	GND	Ground	N/A
D19	GND	Ground	N/A

Table 2– 29. PC/104-Plus Expansion Bus Connector, P3 (A1-D30)

Pin	A	B	C	D
1	GND/5.0V KEY <sup>4</sup>	Reserved	+5	AD00
2	VI/O (+5V)	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O (+5V)	AD10	M66EN <sup>1</sup>
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O (+5V)	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O (+5V)	GNT2*	GND
26	+5V	CLK0	GND	CLK1F
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY <sup>4</sup>

## PCI Bus (P3) Notes

1. Signal M66EN is grounded on the motherboard (Ground = 33MHz bus speed).
2. The shaded cells in the table denote unsupported signals.
3. The KEY pins are to guarantee proper module installation. Pin-A1 is removed and the female side plugged for 5.0V I/O signals. 3.3V PCI I/O signals are not supported.

## Configuration Jumper W1

There is a single configuration jumper on the CoreModule/P5e. It is used to provide an enable signal to an External BIOS Board. The External BIOS Board is only used to recover from a failed BIOS upgrade or to develop a new BIOS. See the section below on BIOS Recovery for information on using the External BIOS Board.

For normal operation, install a jumper on W1. This enables the on-board BIOS. Remove this jumper only when you attach an External BIOS Board.

## Setup

Many options provided on the CoreModule/P5e are controlled by the Setup function. The parameters are displayed on several screens, selected from a main menu screen. To configure the board, you modify the fields in these screens and save the results in the on-board *configuration memory*.

The configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and an Ampro-unique configuration EEPROM. To enhance embedded-system reliability, the contents of the EEPROM mirror the contents of the CMOS memory. The EEPROM retains your configuration information even if the clock's backup battery fails.

The Setup information is retrieved from configuration memory when the board is powered up or when it is rebooted with a CTL-ALT-DEL key combination. Changes made to the Setup parameters (with the exception of the real-time clock time and date settings) do not take effect until the board is rebooted.

The Setup function is located in the ROM BIOS. It can be accessed by pressing DEL while the computer is in the Power On Self Test (POST), just prior to booting. This is called *hot key* access. The screen will display a message indicating when entering DEL will access Setup.

Some Setup fields, for example, the amount of DRAM memory installed on the board, are read-only fields, intended for informational purposes only.

The figures that follow are samples of what the BIOS Setup Pages look like. They may not exactly match your setup screen.

### Setup Help

You can access help information for many of the Setup options by pressing F1. The information is displayed in a popup window. Some help screens list all the available option settings, while others display additional information.

Table 2-30 summarizes the choices found on each Setup page.

*Table 2– 30. Functions on Each Setup Page*

Page	Menu Name	Functions
1	Main Menu	Select various Setup screens Load BIOS or Setup defaults Configure IDE auto detection Save and/or Exit Setup
2	Standard CMOS Setup	Set date and time Enter IDE hard disk parameters Set type and number of floppy disks Set default video state Configure BIOS error handling Displays amount of installed DRAM memory

Table 2– 30. Functions on Each Setup Page (cont.)

Page	Menu Name	Functions
3	BIOS Features Setup	Enable/disable virus warning message Enable/disable internal CPU cache Enable/disable quick POST Additional floppy parameters Set NumLock default state Configure keyboard typematic rates Enable/disable PCI/VGA palette snoop Select OS for DRAM > 64MB Enable/disable system status messages Enable/disable shadowing of memory areas Enable/disable Disk-On-Chip Enable/disable watchdog timer (30s, 60s, 90s) Enable/disable serial console Enable/disable boot loader
4	Chipset Features Setup	Configure memory timing (not recommended)
5	Power Management Setup	Enable/disable power management features Set power management level Set power management options Set power management timers Select power management events
6	PCI Configuration Setup	IRQ configuration IDE interrupt configuration
7	Integrated Peripherals Setup	Enable/disable/configure IDE interfaces Enable/disable support for USB keyboard Enable/disable floppy disk controller Enable/disable/configure serial ports Configure IrDA port Enable/disable/configure parallel port Configure support for MiniModule/ESB devices

## Setup 1 — Main Menu

The first Setup page contains a menu for accessing several Setup screens, plus several additional parameters. Figure 2- 4 shows Setup page 1. Sections following the figure describe each option.

CMOS SETUP UTILITY Ampro Computers, Inc.	
STANDARD CMOS SETUP BIOS FEATURES SETUP CHIPSET FEATURES SETUP POWER MANAGEMENT SETUP PCI CONFIGURATION SETUP INTEGRATED PERIPHERALS	LOAD BIOS DEFAULTS LOAD SETUP DEFAULTS IDE HDD AUTO DETECTION SAVE & EXIT SETUP EXIT WITHOUT SAVING
ESC : Quit    ↑ ↓ → ←    : Select Item F1 : Help    (Shift)F2 : Change Color	
Help messages for each feature line appear here	

Figure 2- 4. Setup 1 — Main Menu

The main menu screen allows the selection of other optional setup screens.

- **STANDARD CMOS Setup** — allows the setup of time, date, hard and floppy disk, and POST halt conditions.
- **BIOS FEATURES Setup** — selects BIOS features including Virus Warning, caching, POST speed, boot sequence, floppy features, default NumLock state, keyboard typematic selection, PCI/VGA palette snoop, system status display, shadowing, D000 segment usage, onboard DOC 2000, watchdog timer, serial console, and serial boot loader.
- **CHIPSET FEATURES Setup** — allows you to modify chipset functions, including configuration, DRAM timing, refresh, ISA bus timing, memory allocation at 15M, PCI version compliance, and BIOS cacheability.
- **POWER MANAGEMENT Setup** — selects and configures power management features.
- **INTEGRATED PERIPHERALS SETUP** — allows the setup of the IDE interface and mode support, configuration of the floppy, serial, parallel, and USB interfaces, and configuration of MiniModule/ESB interfaces.
- **LOAD BIOS DEFAULTS** — sets all BIOS features to a predefined power-on default state.
- **LOAD Setup DEFAULTS** — initializes all chipset features to the default state.
- **IDE HDD AUTO DETECTION** — polls the IDE interfaces for hard disks and displays the various ways the device can be configured.
- **SAVE & EXIT SETUP** — prompts to save CMOS information and exits.
- **EXIT WITHOUT SAVING** — exits without writing Setup information.

## Setup 2 — Standard CMOS Setup

Use Setup 2 to set the date and time, configure your hard and floppy disks, and report system memory. Figure 2- 5 shows what can be configured on Setup 2, and the sections that follow describe each parameter.

STANDARD CMOS Setup									
Ampro Computers, Inc.									
Date (mm:dd:yyyy) : Wed, Feb 23, 1997									
Time (hh:mm:ss) : 8 : 17 : 25									
<hr/>									
HARD DISK	TYPE	SIZE	CYLS	HEAD	PRECOMP	LANDZ	SECTOR	MODE	
Primary Master	: Auto	0	0	0	0	0	0	AUTO	
Primary Slave	: Auto	0	0	0	0	0	0	AUTO	
<hr/>									
Drive A	: 1.44M, 3.5 in.				Base Memory:	640K			
Drive B	: None				Extended Memory:	7168K			
					Other Memory:	384K			
Video	: EGA/VGA				<hr/>				
Halt On	: All Errors				Total Memory:	8192K			
<hr/>									
ESC : Quit:	↑ ↓ → ← : Select Item				PU/PD/+/- : Modify				
F1 : Help	(Shift)F2 : Change Color								

Figure 2- 5. Setup 2 — Standard CMOS Setup

This Setup screen allows you to configure the following parameters:

- **DATE** and **TIME** — requires the numeric entry of *mm:dd:yyyy*. (Note full 4 digit year.) Day of the week and calendar month are displayed. Time and date entries take effect as soon as they are entered.
- **HARD DISK** — set the parameters for the drives connected to the IDE interface. (No parameters are displayed for an auto-detected HD.) When Auto TYPE is used, the MODE should also be AUTO. See “IDE Hard Disk Drives” below for more information.
- **FLOPPY DISK** — select the type of floppy drive(s) connected to the floppy drive interface. See “Floppy Drives” below for more information.
- **VIDEO** — select the initial video mode. See “Video” below for more information.
- **HALT ON** — select the Power On Self Test (POST) response to errors. See “Error Halt” below for more information.
- **Base Memory, Extended Memory, Other Memory** — displays the amount of memory detected by the BIOS. Other Memory reports memory used for ROM shadowing the system BIOS, video BIOS, SCSI BIOS, and any other system extensions. It is not available for general OEM use. See “DRAM Memory” below for more information.

### EIDE Hard Disk Drives

The module supports up to two hard disk drives connected to the IDE interface. Only hard disk drives are directly supported in the system’s ROM BIOS. IDE CD-ROM drives and other IDE-interfaced peripherals are configured by software or drivers supplied separately.

Physical drives can have one or more logical partitions. You can install up to eight logical drives using drive partitions.

To configure the system for the IDE hard drives in your system, set the drive parameters with Setup, as outlined here:

- **Drive Types** — the configuration memory contains a default list of parameters that specify the physical format of each drive. Each *type* specifies the total number of cylinders, number of heads, cylinder to begin precompensation, landing zone cylinder number, and the number of sectors per cylinder. The drive manufacturer supplies these parameters. The list contains “legacy values”, standard for PCs — a number of older (smaller) drives are defined.

Drive type **USER** lets you enter drive parameters manually. If no built-in drive type matches your drive, select drive type USER and enter the drive parameters in the fields provided.

Drive type **AUTO** selects **Autoconfigure**. Autoconfigure queries the drive for its parameters. Most modern drives will respond to the query, allowing the BIOS to set the drive parameter values automatically. This option also provides Logical Block Addressing (LBA) capability, which is used to support drives larger than 512M bytes.

#### Note

---

LBA uses a translation scheme to convert physical heads, sectors and cylinders to logical block numbers. Due to differences in the translation schemes used by different system BIOSes, LBA-compatible drives that have been formatted on Ampro systems may not function properly in other systems that support LBA mode. However, due to the intelligent translation algorithm in the Ampro BIOS, drives formatted in other systems are likely to be usable on the CoreModule/P5e CPU. Note that this only applies to IDE drives that support LBA mode. Consult the technical literature for the drive you select to find out if it supports LBA mode.

---

#### *Drive Selection*

Besides specifying the physical characteristics of each IDE drive, you must also specify whether a drive is a *master* or *slave* drive. The first drive in a system is always configured as a master drive. A second drive would be a slave drive. Each manufacturer may use a different scheme to handle the master and slave relationship, so drives from different manufacturers may not be compatible. Be sure to test drive compatibility in systems with two IDE drives.

Drives default to master from the factory, so if you only have one IDE drive in a system it is generally already set up properly.

Once you have set the system’s configuration memory, the IDE drive(s) can be formatted and otherwise prepared normally. Refer to your operating system and disk drive documentation for specific procedures and requirements.

## Floppy Drives

The ROM BIOS supports all of the popular DOS-compatible floppy disk formats. This includes all the 5-1/4 inch and 3-1/2 inch floppy formats — 360K, 720K, 1.2M, and 1.44M.

### *Drive Parameter Setup*

Enter the number and type of floppy drives in the system. If the drives connected to the system do not match the parameters in the configuration memory, POST displays an error message. To eliminate the error message, set the drive parameters to match your floppy drives.

## Video

Specify the initial video mode. Select **Mono**, **CGA40**, **CGA80**, or **EGA/VGA**. If your video display card is VGA, super VGA, or any other high resolution standard, specify **EGA/VGA** no matter how it is configured to come up.

## Error Halt

Select which kinds of errors will halt the Power-On Self Test (POST). If you plan to use the module without a keyboard, be sure to set this option to *not* halt on keyboard error.

## DRAM Memory

The ROM BIOS automatically detects the amount of memory during POST and stores the result when you save the configuration values when exiting Setup. This Setup page displays the amount of memory found in the system.

## Setup 3 — BIOS Features Setup

Use Setup 3 to set a variety of BIOS feature options. Figure 2- 6 shows what can be configured on Setup 3, and the sections that follow describe each parameter.

BIOS FEATURES Setup Ampro Computers, Inc.	
Virus Warning : Disabled CPU Internal Cache : Enabled Quick Power On Self Test : Disabled Boot Sequence : A,C Swap Floppy Drive : Disabled Boot Up Floppy Seek : Enabled Boot Up NumLock Status : Off Typematic Rate Setting : Disabled Typematic Rate (chars/Sec) : 6 Typematic Delay (Msec) : 250 PCI/VGA Palette Snoop: : Disabled OS Select For DRAM > 64MB : Non-OS2 Show System Status at Boot : Enabled	Video BIOS Shadow : Enabled D000 Segment Usage : NAND BIOS Extnsn On-Board DOC 2000 : Enabled Serial Console : Disabled Serial Boot Loader : Disabled
ESC:Quit                   ↑ ↓ → ← :Select Item F1 :Help                    PU/PD/+/- :Modify F5 :Old Values (Shift)F2 :Color F6 :Load BIOS Defaults F7 :Load Setup Defaults	

Figure 2– 6. Setup 3 — BIOS Features Setup

This Setup screen allows you to configure the following parameters:

- **Virus Warning** — monitors for writes to the hard disk boot sector. If a write is detected, the BIOS will display the following warning message, beep the speaker, and wait for user confirmation.

```

!!! WARNING !!!
Disk Boot sector is to be modified
type "Y" to accept, any key to abort
Award Software, Inc.
```

- **CPU Internal Cache** — enable or disable the 16K Pentium internal cache.
- **Quick Power On Self Test** — when enabled, the POST will skip some non-essential tests (such as repetitive memory tests) in order to shorten the POST time.
- **Boot Sequence** — determines the order in which drives should be searched by the disk operating system. Options are [A, C], [C, A], [A, SCSI], [SCSI, A], [CD, A, C], [C only], and [SCSI only]. ("C" refers to an IDE drive, and "CD" refers to an IDE CD-ROM drive.)
- **Swap Floppy Drive** — If two floppy drives are connected to the system, drive A becomes drive B and vice-versa.
- **Boot Up Floppy Seek** — during POST, the BIOS performs a seek test to determine if the drive is 40 or 80 tracks (360K drives have 40 tracks, other drives have 80 tracks).

- **Boot Up NumLock Status** — sets the default state of the keyboard's numeric keypad. **On** sets the keypad to numbers, **Off** sets the keypad to arrows.
- **Typematic Rate Setting** — enable or disable the typematic function (automatic keyboard key repeat).
- **Typematic Rate (chars/S)** — set the typematic rate. This is the rate at which a held-down key is repeated.
- **Typematic Delay (mS)** — set the time a key must be pressed before typematic repeating begins.
- **PCI/VGA Palette Snoop** — enables PCI- or ISA-based graphics adapters which are not VGA-compatible to monitor writes to the VGA palette registers so they may update their own palette registers accordingly. Note that when PCI/VGA Palette Snoop is enabled, graphic screens may be distorted when booting Windows 95.
- **OS Select for DRAM > 64MB** — if you are running OS/2, set to **OS/2**. Otherwise set to **Non-OS/2**. This parameter limits reporting memory above 64 MB, as some operating systems fail when more than 64 MB is reported. Some versions of OS/2 have this problem.
- **Show System Status at Boot** — when enabled (the default), some messages about detected hardware features are displayed on the console during the Power-On Self Test.
- **Shadow Options** — determines whether option ROMs in the specified address range are shadowed in DRAM. PCI devices with on-board ROM are always shadowed. These are not affected by this setting.
- **D000 Segment Usage** — specifies how the D0000 - DFFFF memory segment is allocated. The options are: **Available**, **Shadow RAM**, and **NAND BIOS Extnsn**. The NAND BIOS Extension option supports a BIOS extension image installed in the NAND Flash device. For information on installing a BIOS Extension in the NAND Flash device, see the section below on Utility Software.
- **Onboard DOC 2000** — enables or disables the on-board Disk-On-Chip 2000 device.
- **Serial Console** — enables or disables use of a serial console connected to a serial port. When used as a serial console, the serial port does not appear in the BIOS COM port table. This means that it will not be COM1, COM2, etc. Select the serial port and its BAUD rate, such as **Serial 1@2400**, **Serial 2@9600**, and so forth. Other communication parameters are fixed at 8-bit words, 1 start bit, 1 stop bit, and no parity. Default setup of the serial console port is **Disabled**.
- **Serial Boot Loader** — enables or disables the serial boot loader function. When you enable the boot loader, select either **COM1 or COM2**. Other communication parameters are fixed at 9600 BAUD, 8-bit words, 1 start bit, 1 stop bit, and no parity.

## Serial Console Operation During Setup

When Setup is being run using the serial console interface, keyboard arrow keys and function keys must be simulated. The following simulations are used for these keys:

**Arrow Keys** — arrow keys may be entered as shown on the screen. Use the following substitutes for the arrow keys. Note that there are both standard keys and control key sequences for each command:

<b>^, Ctrl-e</b>	Up arrow	<b>&gt;, Ctrl-d</b>	Right arrow
<b>v, Ctrl-x</b>	Down arrow	<b>&lt;, Ctrl-s</b>	Left arrow
<b>Ctrl-r</b>	Page up	<b>Ctrl-c</b>	Page down

Note that these keys simulate the arrow keys only during Setup, not during normal computer operation.

**Function Keys** — function keys (F1, F2, etc.) are entered with two keystrokes. The first entry is “F”, followed by the number. F10 is simulated by typing “F” and then “0”.

Note that these keystrokes simulate the function keys only during Setup, not during normal computer operation.

## Setup 4 — Chipset Features Setup

Setup 4 — Chipset Features Setup controls internal chipset features. **Many of these items should never be changed by the OEM or end user, as they specify internal parameters that have been chosen to support the existing motherboard design.** Change these parameters only if directed to by Ampro Technical Support. Figure 2- 7 shows what can be configured on Setup 4. The items that can be changed by the OEM are listed below.

Chipset Features Setup Ampro Computers, Inc.	
Auto Configuration	: Enabled
DRAM Timing	: 70ns
DRAM Leadoff Timing	: 10/6/4
DRAM Read Bursts (EDO/FP)	: x333/x444
DRAM Write Burst Timing	: x333
Fast EDO Lead Off	: Disable
Refresh RAS# Assertion	: 5 Clks
Fast RAS To CAS Delay	: 3
DRAM Page Idle Timer	: 2 Clks
DRAM Enhanced Paging	: Enabled
Fast MA to RAS# Delay	: 2 Clks
System BIOS Cacheable	: Disabled
Video BIOS Cacheable	: Disabled
8-bit I/O Recovery Time	: 1
16-Bit I/O Recovery Time	: 2
Memory Hole At 15M-16M	: Disabled
PCI 2.1 Compliance	: Disabled
ESC:Quit    ↑ ↓ → ←    : Select Item F1 :Help    PU/PD/+/-    : Modify F5 :Old Values    (Shift)F2:Color F6 :Load BIOS Defaults F7 :Load Setup Defaults	

*Figure 2– 7. Setup 4 — Chipset Features Setup*

This Setup screen allows you to configure the following parameters:

- **Auto Configuration** — if enabled, the DRAM timing selection of 70 nS or 60 nS automatically configures the following five RAM timing parameters. If disabled, these parameters must be configured manually. This option should be left in its default state. Contact Ampro Technical Support or your Ampro Sales Representative for advice if you have unique requirements that require changing these parameters.
- **System and Video BIOS Cacheable** — these options allow BIOS code to be cached in the CPU.
- **8- and 16-Bit I/O Recovery Time** — these options allow additional delays to be inserted between PCI-initiated I/O transactions to the ISA bus. Options are 1 to 8 clocks, or NA, for no additional delays.
- **Memory Hole at 15M-16M** — certain peripheral adapters may require memory in the 15M-16M address range. The memory hole option creates a 1 MB memory hole below the 16 M boundary for this purpose.
- **PCI 2.1 Compliance** — this parameter controls the timing of certain PCI bus transactions. Select Enabled only if all PCI devices in the system are known to be compliant with Version 2.1 of the PCI specification.

## Setup 5 — Power Management Setup

The CoreModule/P5e CPU BIOS incorporates power management features compliant with Advanced Power Management (APM) BIOS Interface Specification Revision 1.1, created by Intel and Microsoft. Setup 5 — Power Management Setup allows you to configure your system to most effectively save energy while operating at the speed and response level you need in your application. Figure 2- 8 shows what can be configured on Setup 5. A description of each option is listed below.

### Note

When features of the APM BIOS are enabled, some reduced power states are entered automatically. Reduced power states alter the performance of the system, usually slowing or halting the CPU. Use the power management functions with care when using the CoreModule in applications which require guaranteed maximum response times.

POWER MANAGEMENT Setup Ampro Computers, Inc.		
Power Management	:Disabled	** Reload Global Timer Events **
PM Control by APM	:Yes	IRQ[3-7,9-15],NMI :Disabled
Video Off Option	:Always On	IDE Hard Disk 0 :Disabled
		IDE Hard Disk 1 :Disabled
		Floppy Disk :Disabled
Doze Mode	:Disabled	Serial Port :Enabled
Standby Mode	:Disabled	Parallel Port :Disabled
Suspend Mode	:Disabled	
HDD Power Down	:Disabled	
Throttle Duty Cycle	:62.5%	
VGA Active Monitor	:Enabled	
Resume By Ring	:Disabled	
** Break Event From Suspend **		
IRQ 8 Clock Event	:Disabled	
		ESC:Quit ↑ ↓ → ← : Select Item
		F1 :Help PU/PD/+/- : Modify
		F5 :Old Values (Shift)F2:Color
		F6 :Load BIOS Defaults
		F7 :Load Setup Defaults

Figure 2– 8. Setup 5 — Power Management Setup

This Setup screen allows you to configure the following parameters:

- **Power Management** — sets the type or degree of power savings and is directly related to the power management modes defined by the APM specification. Settings are **Disable** (default), **Min. Savings**, **Max. Savings**, and **User Defined**. The difference between Min and Max Savings is the time delay period between modes.

- **PM Control by APM** — when enabled, it allows operating systems with power management support to control the modes required for safe operation of shutdown occurrences.
- **Video Off Option** — sets the conditions under which the BIOS powers down the video (assuming your video interface supports power management). Select the **DPMS** option only if your monitor supports the VESA Display Power Management Signaling standard. **H/H SyNC+Blank** turns off the horizontal and vertical sync signals and blanks the video buffer. **Blank Screen** only blanks the video buffer.

The power management timers are only configurable if the **Power Management** option is set to **User Defined**. Each timer sets the amount of idle time before the system enters the specified power-saving mode. These modes are:

- **Doze Mode** — when enabled and after a set time of system inactivity, the CPU clock speed is reduced. Other devices remain active.
- **Standby Mode** — when enabled and after a set time of system inactivity, the CPU clock speed is reduced, and the disk drives and video monitor are shut down. Other devices remain active.
- **Suspend Mode** — when enabled and after a set time of system inactivity, all activities except DRAM refresh are shut down.
- **HDD Power Down** — when enabled and after a set time of system inactivity, the hard disk drives are shut down. All other devices remain active.
  
- **Throttle Duty Cycle** — selects a percentage of time the CPU runs in Doze Mode.
- **VGA Active Monitor** — when enabled, any video activity restarts the Standby Mode timer.
- **IRQ Clock Event** — when enabled, a real-time clock interrupt will awaken the system from Suspend Mode.
- **Reload Global Timer Events** — any of the Reload Global Timer Events will cause the Standby Mode timer to be restarted when the event is detected.

## Setup 6 — PCI Configuration Setup

The CoreModule/P5e CPU BIOS incorporates automatic PCI IRQ configuration for peripherals. You can, however, override the automatic features and specify PCI IRQ settings with SETUP 6. Figure 2- 9 shows what can be configured on SETUP 6. A description of each option is listed below.

PCI CONFIGURATION SETUP Ampro Computers, Inc.	
1st Available IRQ	:10
2nd Available IRQ	:11
3rd Available IRQ	:9
4th Available IRQ	:5
PCI IDE IRQ Map To	:PCI-AUTO
PCI IRQ INT# Pin	:A
ESC:Quit           ↑ ↓ → ← : Select Item F1 :Help            PU/PD/+/- : Modify F5 :Old Values    (Shift)F2:Color F6 :Load BIOS Defaults F7 :Load Setup Defaults	

Figure 2- 9. SETUP 6 — PCI Configuration Setup

This SETUP screen allows you to configure the following parameters:

- **Nth Available IRQ** — selects the order in which ISA IRQ channels can be assigned to PCI devices.
- **PCI IDE Options** — these options must be left in their default state.

## Setup 7 — Integrated Peripherals Setup

The peripheral interfaces integrated on the CoreModule/P5e can be configured on Setup 7 — Integrated Peripherals Setup. You can configure the IDE port, USB port, floppy controller, IrDA port, serial ports, and parallel port from this screen.

INTEGRATED PERIPHERALS SETUP Ampro Computers, Inc.	
IDE HDD Block Mode	:Enabled
IDE Master PIO Mode	:Auto
IDE Slave PIO Mode	:Auto
IDE Master Ultra DMA	:Disabled
IDE Slave Ultra DMA	:Disabled
On-Board IDE Controller	:Enabled
On-Board FDC Controller	:Enabled
On-Board UART 1	:3F8/IRQ4
On-Board UART 2	:2F8/IRQ3
UART2Rx Signal Polarity	:Normal
UART2Tx Signal Polarity	:Normal
On-Board UART 2 Mode	:Standard
IR Duplex Mode	:Half
Use IR Pins	:IR-RX2TX2
Onboard Parallel Port	:378/IRQ7
Parallel Port Mode	:Normal
ECP Mode use DMA	:3
Parallel Port EPP Type	:EPP1.7
Use IR's IRQIN Pins	:IRR3 (IR Mode)
ESC:Quit      ↑ ↓ → ← : Select Item F1 :Help                    PU/PD/+/-: Modify F5 :Old Values            (Shift)F2:Color F6 :Load BIOS Defaults F7 :Load Setup Defaults	

Figure 2– 10. SETUP 6 — PCI Configuration Setup

- **IDE HDD Block Mode** — when enabled, this allows your hard drive system to use a mode where the interface transfers large blocks of data instead of the normal small blocks. **Enabled** is the default state, and works for newer hard drives. Disable this feature if your drive does not support block mode transfers.
- **IDE Master/Slave PIO Mode** — sets the PIO mode for devices attached to the IDE interface. **Auto** (default) lets the BIOS automatically determine what mode is fastest for each device. **Mode 1** through **Mode 4** forces the BIOS to use the specified mode, and overrides the MODE setting on the Standard CMOS Setup Screen, Setup 2.
- **IDE Master/Slave Ultra DMA** — enable or disable support for Ultra DMA/33 mode on the selected IDE device. When set to “AUTO”, Ultra DMA/33 will be used if it is supported by the connected IDE drive.
- **On-board FDC Controller** — enables or disables the on-board floppy disk controller.
- **On-board UART *n*** — configures each serial port’s address and interrupt. Available choices for the I/O addresses are 3F8, 2F8, 3E8, and 2E8. Available IRQ choices are IRQ3 and IRQ4. If you select Auto, the BIOS makes the choices for you. You may also disable either port.
- **On-Board UART 2 Mode** — configures the second serial port to be a standard serial port or for one of the IrDA modes. Enabling one of the IrDA modes provides access to the IR

configuration parameters. Available IrDA modes are HPSIR (standard IrDA), ASKIR (amplitude shift keyed infrared), fast IR, or TTL.

- **IR Duplex Mode** — select full or half duplex IR operation. Your choice will depend on what IR device you are using in your system.
- **Use IR Pins** — selects which transmit and receive pins to use with the IR interface. Your IR interface specification should tell which Tx and Rx pins to use.
- **On-board Parallel Port** — set the parallel port address and IRQ assignments. Available addresses are 378, 278, or 3BC. Available IRQ assignments are IRQ 7 and IRQ5. You may also disable the port.
- **Parallel Port Mode** — set the parallel port mode, either **Normal**, **EPP**, **ECP**, or **EPP/ECP** as shown in Table 2-31.

Table 2– 31. Parallel Port Modes

Option	Selected Mode
Normal	Standard parallel port (default)
EPP	Bi-directional mode
ECP	Fast, buffered, IEEE-1284
EPP/ECP	Bi-directional and buffered

- **ECP Mode Use DMA** — selects a DMA channel (1 or 3) to use with the ECP mode of the parallel port. This selection only applies if the parallel port is configured for ECP or EPP/ECP modes.
- **Parallel Port EPP Type** — configures the parallel port to comply with EPP specification version 1.7 or 1.9 when in EPP mode. This selection only applies if the parallel port is configured for ECP or EPP/ECP modes.

## CoreModule/P5e specific Utility Software:

Four utilities are supplied on the CoreModule/P5e Utility Disk. This section will discuss the use of these utilities. Additional software utilities are provided on the Common Utilities Disk. See the Common Utilities Technical Manual for documentation on these other utilities.

Three of the software utilities on this CoreModule/P5e Utility Disk are used to format and program the NAND Flash device found on the optional NAND version of the CoreModule/P5e. This non-volatile NAND flash memory contains the CPU BIOS, a flash file system, and optional BIOS Extensions. The fourth utility is used on the zero NAND version.

### NAND FLASH VERSION OF CoreModule/P5e UTILITIES (P5FORMAT.EXE, P5UPDATE.EXE, DINFO.EXE)

When power is applied to the CPU, the BIOS is moved from the NAND Flash device into high speed DRAM for execution. If the BIOS must be updated in the field, or the user wishes to install a BIOS Extension, use of these utilities is required.

---

#### Note

---

The P5FORMAT.EXE, P5UPDATE.EXE, and DINFO.EXE utilities are exclusively for use on the NAND flash version of the CoreModule/P5e. If you have the Zero NAND flash version, please do NOT use them; Instead, use PGMCM5E, described later in this document

---

In the NAND flash version of CoreModule/P5e, a portion of the NAND Flash device may be utilized as non-rotating mass storage media. It can be made to emulate an M-Systems DiskOnChip® 2000. The CoreModule/P5e NAND flash comes with a NAND Flash device. A portion of the device is used to store the True Flash File System (TrueFFS®) firmware from M-Systems. Use of the DiskOnChip feature is enabled or disabled on Setup screen 3.

The NAND Flash may also be used to store a BIOS Extension provided by the user. This mode needs to be enabled in Setup as described in the section above on Setup screen 3. If enabled, the CoreModule/P5e will search for the BIOS extension during the BOOT process. If an extension is found (the BIOS extension must start with 55AA to be recognized), the code is moved to the D000 segment of the system DRAM. The code may be any size up to 64K, but it cannot be greater than 64K. Regardless of its size, a 64K block of the NAND Flash is reserved to store the image. (For more information about BIOS support, contact AMPRO Technical Support.)

---

**WARNING**


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Do NOT use the standard M-Systems utilities 'DUPDATE.EXE' and 'DFORMAT.EXE' for operations on the on-board DiskOnChip 2000. These utilities are NOT compatible with the CoreModule/P5e.

---

## P5FORMAT.EXE

P5FORMAT is used on the NAND flash version of CoreModule/P5e to initialize and prepare the NAND Flash device for use as a general purpose storage device. Command line switches also load the TrueFFS firmware, the Ampro CPU BIOS, and an optional BIOS Extension into the device at reserved locations. P5FORMAT will also create a DOS partition on the Flash device, and create a root directory.

---

**Note**


---

Any files in a previously formatted file system will be lost when P5FORMAT is run.

---

If enabled in Setup screen 3, the next time the CPU is Booted, the BIOS will install this area as a hard disk drive.

The NAND version of the CoreModule/P5e is shipped from the factory with a formatted Flash device. The default format does not reserve space for a BIOS extension (using the /BEXT switch). Consequently, if you wish to install a BIOS extension, it will be necessary to reformat the device using the P5FORMAT utility and the /BEXT switch. This reformatting only needs to be done once to repartition the flash device and to reserve a 64K block for the BIOS extension. You can then use the P5UPDATE utility to update the BIOS extension image. Under most other scenarios, you should not have to use P5FORMAT. However, if the NAND Flash device contents are overwritten with bad data, this utility can be used to recover the device. If the CoreModule/P5e CPU will not BOOT because of problems with the Flash device, there is boot ROM support for the CoreModule which can be used to recover the BIOS. See the section below on BIOS Recovery.

The syntax of the P5FORMAT.EXE command is:

```
>C: P5FORMAT {/WIN:e000} {/S:filenam1.exb} {/BIPO:filenam2.bin}
      [/BEXT:filenam3.bin] [/FIRST] [/Y]
```

Switches:

- `/WIN:e000` Required. Memory Address of the NAND Flash device.
- `/S:filenam1.exb` Required. Loads filenam1.exb into the DiskOnChip Firmware area.
- `/BIPO:filenam2.bin` Required. Loads filenam2.bin into the CPU BIOS area.
- `/BEXT:filename3.bin` Optional. Loads filename3.bin into the BIOS Extension area.
- `/FIRST` Optional. Causes the DiskOnChip to be the first disk in the system (C:).  
Default is  
last disk. This switch has no effect if the DiskOnChip is the only disk in the system.  
The `/S` flag must be used in conjunction with the `/FIRST` switch.
- `/Y` Optional. Do not pause for confirmation before writing BIOS image.

The `/WIN:`, `/S:`, and `/BIPO:` switches are required. The `/BEXT:` switch should only be used when BIOS Extension code is to be installed on the NAND Flash device. After the command line is entered, P5FORMAT will sign on. As a precaution against accidentally formatting the Flash device, P5FORMAT will ask twice for confirmation of the format request (if the `/Y` switch is not used).

The first query requires 'y' to be entered. The second confirmation request requires the password "BIPO" to be entered. All commands and switches are not case-sensitive. P5FORMAT will then begin to format the Flash device.

After the format process is complete, the DiskOnChip firmware and the BIOS image (and optionally the BIOS Extension) are written to the flash device. If the DiskOnChip is to be the BOOT device, you must use the DOS SYS command to copy the DOS file system software to the DiskOnChip. You may then re-boot the CPU to execute the new firmware.

---

## P5UPDATE.EXE

P5UPDATE.EXE is similar to P5FORMAT.EXE, except that it does not format the NAND Flash device. It is used to update the CPU BIOS, TrueFFS firmware, or the optional BIOS Extension code. The Flash device must already be formatted when P5UPDATE is used.

Note that you cannot use P5UPDATE to install a BIOS extension if the NAND flash does not already have a 64K block already reserved. You will need to re-run P5FORMAT using the `/BEXT` switch in order to allocate space for the BIOS extension. Subsequent updates to the BIOS extension code can then be performed using P5UPDATE.

The syntax of the P5UPDATE.EXE command is:

```
>C: P5UPDATE {/WIN:e000} [/S:filenam1.exb] [/BIPO:filenam2.bin] [/BEXT:filenam3.bin]
    [/FIRST] [/Y]
```

Switches:

/WIN:e000	Required. Memory Address of the NAND Flash device.
/S:filenam1.exb	Optional. Loads filenam1.exb into the DiskOnChip Firmware area.
/BIPO:filenam2.bin	Optional. Loads filenam2.bin into the CPU BIOS area.
/BEXT:filenam3.bin	Optional. Loads filenam3.bin into the BIOS Extension area.
/FIRST Default	Optional. Causes the DiskOnChip to be the first disk in the system (C:). is last disk. This switch has no effect if the DiskOnChip is the only disk in the system. The /S flag must be used in conjunction with the /FIRST switch.
/Y for	Optional. If the switch /BIPO: is used, /Y will cause P5UPDATE not to pause for confirmation before writing BIOS image.

For P5UPDATE, the /WIN: switch is required. The other switches may be used separately or in any combination, except if the /FIRST: switch is used, the /S: switch must also be used. After the command line is entered, P5UPDATE will sign on. As a precaution against accidentally overwriting BIOS in the Flash device, P5UPDATE will ask for confirmation of the request. Enter "BIPO" and press return. P5UPDATE will then begin the BIOS update process.

After the update process is complete, you may then re-boot the CPU to execute the new firmware.

-----

**DINFO.EXE**

DINFO.EXE is a utility that will examine the NAND Flash device and report certain parameters. This utility has no switches. Running this utility on a CoreModule/P5e with a NAND Flash device will yield a screen similar to the one shown here:

DINFO Version 3.3.7 for DiskOnChip 2000 (V1.10)

Copyright (C) M-Systems, 1992-1998

DiskOnChip 2000(R) found at E000:0000

-----  
Disk Statistics:

Drive letter : C

Disk size : 3824 Kbytes

Software version : 1.07

TrueFFS Compatibility: 3.3.02

Firmware size : 176 Kbytes

-----  
UTILITY FOR THE ZERO NAND VERSION OF THE CoreModule/P5e

**Note**

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The PGMCM5E.COM utility is used exclusively with the zero NAND flash version of the CoreModule/P5e.

---

## PGMCM5E.COM

This utility is used only for the zero NAND Flash version of the CoreModule/P5e. The Zero NAND Flash version does not store its BIOS on NAND flash, but instead on a 128K Flash device. The BIOS occupies 128K of the flash device, so there is no additional space available for user configuration or BIOS extension on this version.

By typing PGMCM5E /? Or /H, you will get the command line option structure, which is:

PGMCM5E [filename.bin]

Where the 'filename.bin' is the 128K binary BIOS image file.

## BIOS RECOVERY

Despite precautions, there is a possibility that the Core Module/P5e BIOS could become corrupted during the firmware update process. This may occur when an update of the BIOS image fails or inappropriate switch options are used for programming the NAND flash.

Both the NAND flash and Zero NAND versions of the CoreModule/P5e are designed to be recoverable from a damaged BIOS. There is a small portion of the BIOS that is stored either in boot block flash (Zero-NAND) or in a separate flash chip (NAND), depending upon the version that makes recovery of the BIOS possible.

Procedure for recovery of BOTH the Zero NAND version and the NAND version is the same, with only one difference being the utility that is used:

NAND FLASH BIOS RECOVERY: Use P5UPDATE or P5FORMAT.

ZERO NAND BIOS RECOVERY: Use PGMCM5E.

To recover a BIOS:

You will need the following additional items: 1) An ISA or PC/104 video card is required in order to see the update. The small portion of BIOS that is available prior to recovery does not support PCI (or PC/104+) video. The update can still be done without video by using an autoexec type batch file,

but things will go more smoothly if you are able to see video during your recovery. Also 2) A bootable floppy disk with DOS system files on it, and 3) a floppy drive must be attached to your system, as the recovery feature is performed via floppy boot and DOS executable utility.

PROCEDURE

1. Use P5UPDATE or P5FORMAT to recover your NAND flash CoreModule/P5e. (P5FORMAT will erase the contents of the DiskOnChip). Use PGMCM5E to recover your Zero NAND CoreModule/P5e.
2. In either case, you will need the 128K binary BIOS image file. (filename.bin) Copies of CoreModule/P5e BIOS images may be obtained from Ampro Technical Support.
3. Boot the system from floppy drive with an ISA video card
4. Execute the utilities.
5. Restart the system. The CPU should BOOT. (If it does not, the Zero NAND version of CoreModule/P5i should be returned to Ampro for servicing; for the NAND version, there is an additional procedure that can be followed - see the section below on the External BIOS Board).
6. Execute the appropriate utility, including the binary BIOS image file, to reprogram the BIOS on the board.
7. Reboot the system.

The CoreModule should function normally after this procedure.

#### ADDITIONAL NOTE

The BIOS recovery procedure described above will allow you to restore a CoreModule/P5e which has been programmed with an invalid or nonfunctional BIOS image. The CoreModule's boot ROM performs a checksum test on the BIOS during startup to validate the image. If a bad BIOS is detected, a reduced version of POST is executed to start up the system and allow BIOS recovery.

In a development environment, it is also possible for the NAND flash to be programmed with a "good" image (correct checksum) which still prevents the system from booting properly. For example, a BIOS extension being tested for the first time could contain a programming bug that causes the system to hang during startup. This is very unlikely provided that new firmware is tested thoroughly before installation in the NAND flash. However, if it does happen, the system may still be recovered by use of an external BIOS board. Contact Ampro Technical support if you believe that your application may necessitate the purchase of one of these modules.

# Chapter 3

## Technical Specifications

### CoreModule/P5e Specifications

The following section provides technical specifications for the CoreModule/P5e.

#### CPU/Motherboard

- CPU: Mobile Pentium Processor with MMX Technology on 0.25 micron 166 or 266MHz
- System RAM:
  - Sockets for an Ampro custom memory module
  - Supports from 8M bytes to 128M bytes
  - Shadow RAM support provides fast system BIOS execution
- 15 interrupt channels (8259-equivalent)
- 7 DMA channels (8237-equivalent)
- 3 programmable counter/timers (8254-equivalent)
- Standard PC/AT keyboard port
- Standard PC speaker port with .1 watt output drive
- Battery-backed real-time clock and CMOS RAM:
  - Up to 10 year battery life
  - Supports battery-free operation
- Ampro Extended BIOS

#### Embedded-PC System Enhancements

- OEM Flash Memory (optional):
  - On-board programming
  - 8064K available for OEM use
  - Compatible with True Flash File System software and Ampro SSD Support Software, providing “disk-on-chip” functionality (Contact Ampro for details.)
- 4K-bit configuration EEPROM:
  - Stores system Setup parameters
  - Supports battery-free boot capability
  - 512 bits available for OEM use
- Watchdog Timer
  - Timeout triggers hardware reset or NMI
  - 30, 60, 90 second selectable intervals

## On-board Peripherals

This section describes standard peripherals found on every CoreModule/P5e.

- Two buffered serial ports with full handshaking
  - Implemented with 16550-equivalent controllers with built-in 16-byte FIFO buffers
  - On-board generation of RS232C signal levels
  - Logged as COM1 and COM2 by DOS
  - Serial 2 usable as a TTL interface
- IrDA Interface
  - Supports both slow (SIR) and fast (FIR) IrDA specifications
- Two Universal Serial Bus (USB) Ports
  - Supports both slow (115.2K baud) and fast (4 Mbits/sec) USB standards
- Multimode Parallel Port
  - Superset of standard LPT printer port
  - Bi-directional data lines
  - IEEE-1284 (EPP/ECP) compliant
  - Standard hardware supports all four IEEE-1284 protocol modes
  - Internal 16-byte FIFO buffer
  - DMA option for data transfers
- Floppy Disk Controller
  - Supports one or two drives
  - Reliable digital phase-locked loop circuit
  - BIOS supports all standard PC/AT formats: 360K, 1.2M, 720K, 1.44M
- PCI EIDE Disk Controller
  - A PCI bus implementation of an Extended IDE (EIDE) hard disk controller
  - Supports up to two hard disk drives.
  - Fast ATA-capable interface supports high-speed PIO modes
  - BIOS supports drives larger than 528 M bytes through Logical Block Addressing (LBA)
  - Support for Ultra DMA/33 compatible drives

## Mechanical and Environmental Specifications

- Standard PC/104-*Plus* form factor, 3.775 x 3.550 x .6 inches (95.9 x 90 x 15.3 mm). Refer to Figure 2-1 for mounting dimensions.
- Power requirements (typical, with 16M byte DRAM)
  - 166 MHz: 6.1 w
  - 266 MHz: 7.9 w
- Operating environment:
  - 0° to 70° C
  - 5 to 95% relative humidity (non-condensing)
- Storage temperature: -55° to +85° C
- Weight: 4.1 oz. (116 gm), with heatsink and DRAM installed
- ISA portion of the PC/104-*Plus* expansion bus

- Stackthrough, 16-bit bus connectors, for expansion via PC/104 modules
- PCI portion of the PC/104-Plus expansion bus:
  - 4 x 30 (120-pin) 2 mm. pitch stackthrough connector.
  - Electrical specifications equivalent to the PCI Local Bus Specification Rev. 2.1.

## Ampro Product Reliability Testing

### Regulatory testing

Knowing that many embedded systems must qualify under EMC emissions susceptibility testing, Ampro designs boards with careful attention to EMI issues. Boards are tested in standard enclosures to ensure that they can pass such emissions tests. Tests include European Union Directives EN55022 and EN55011 (for EMC), EN61000-4-2 (for ESD), ENV50140 (for RF Susceptibility), and EN61000-4-4 (for EFT). Conducted Emissions testing is also performed at US voltages per FCC Part 15, Subpart J (the European Union Directives are otherwise compatible with Part 15 testing).

### Shock and Vibration Testing

Boards intended for use in harsh environments are tested for shock and vibration durability to MIL-STD 202F, Method 213-I, Condition A (three 50G shocks in each axis) and MIL-STD 202F, Method 214A, Table 214-I, Condition D (11.95B random vibration, 100 Hz to 1000 Hz). (Contact your Ampro sales representative to obtain *Shock and Random Vibration Test Report for the CoreModule/P5e CPU* for details.)

### HALT Testing

The CoreModule/P5e was subjected to Highly Accelerated Life Testing as a part of its Engineering Qualification. HALT testing is used during the development of a product to identify the temperature and vibration Operating Limits and Destruct Limits of the product. The stresses applied to the CoreModule/P5e during this testing were well beyond those expected during normal operation. The intent of the test is to subject the unit to progressively greater extremes of temperature, rapid thermal transitions, vibration (in six axes), and combined temperature and vibration until the unit fails, and then, is ultimately destroyed.

The results of the test identify the elements of the design that are the weakest, and at what level of environmental stress the elements fail or are destroyed. This information is then used to improve the design of the product. The official test report from the third-party lab details the test process, the specific stresses applied, and the observations of the consulting Test Engineer. This test report is available from Ampro Computers, Inc.

### ISO 9001 Manufacturing

Ampro is a certified ISO 9001 vendor.

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# Appendix A

## Cable Specifications

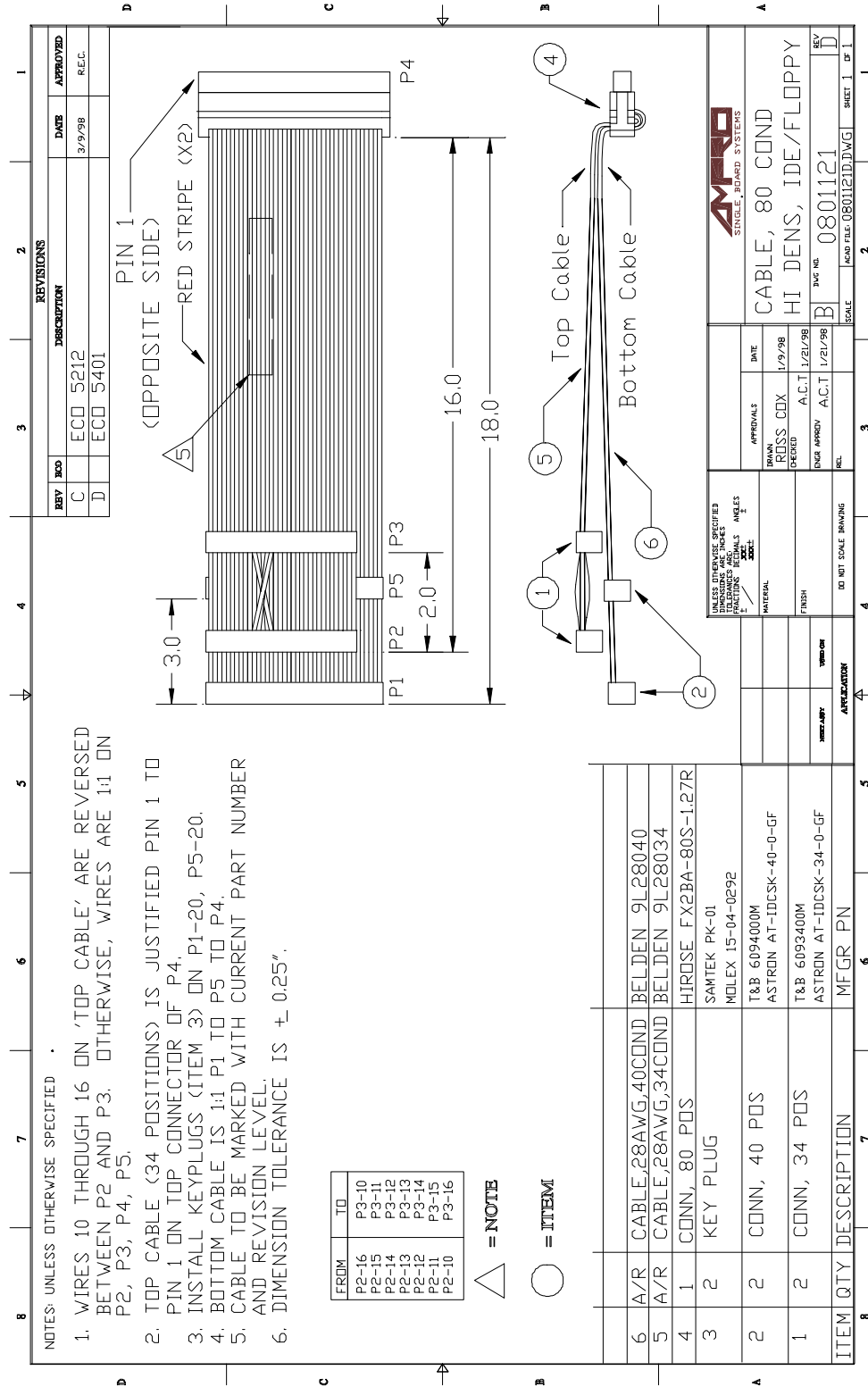


Figure A-1. J4 Cable

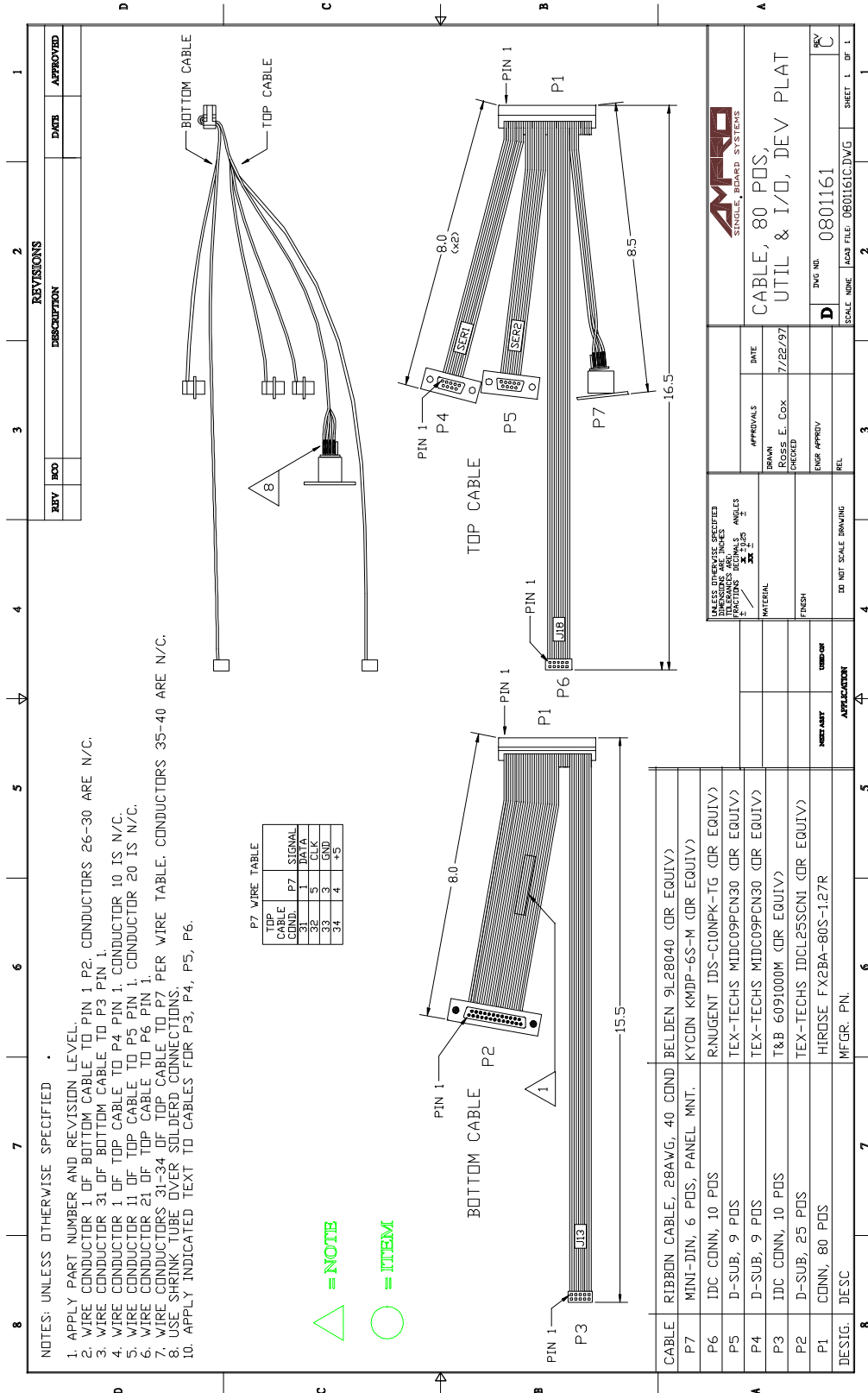


Figure A-2. J5 Cable



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