

Tiny SBC Passes H.A.L.T. for Extremely Rugged Applications

Abstract:

In order to demonstrate the suitability of a single board computer (SBC) for harsh environments including temperature and vibration extremes, a Highly Accelerated Life Test (H.A.L.T.) is performed to uncover any possible latent defects in product design, component selection, and manufacturing process that would not otherwise be found through conventional qualification methods. Ampro's 1 GHz CoreModule™ 800 has risen to the challenge, with successful operation over a -60°C to +90°C range while being subjected to vibration of 50 Grms.

CoreModule 800 reaches 1 GHz

The new 1 GHz CoreModule™ 800 single board computer features Intel's 1 GHz Celeron® M 373 processor along with the 855 chipset in the smallest industry-standard SBC form factor: PCI-104. Fitting a complete embedded computer into only 3.6" x 3.8" and managing the thermal design was no small feat. Ampro achieved a major breakthrough by applying its proven design methodology and robust manufacturing process to hit the target.

Applications

A number of rugged applications require operation in multi-axis shock and vibration, extreme hot and cold, and corrosive environments – all without failures. The CoreModule 800 targets helicopters, trains, airplanes, marine vessels, and military vehicles. HALT reports can be used by electronics system manufacturers in these markets to narrow down the list of SBC suppliers and their products to bring into design and qualification stages of their programs.

Test Purpose

The purpose of the HALT test is to find the potential weak links in product design, to document failure modes, and to determine the true operating and destruct limits. These limits are defined as follows:

- Operating Limit (OL) - The operating limit is defined as the last operational temperature or vibration set point prior to failure.
- Destruct Limit (DL) - The destruct limit is the level at which the product stops functioning and remains inoperable at normal operating conditions.

These limits are measured by using repeatable testing techniques such as thermal step stress, rapid thermal transitions, vibration step stress, and combined temperature and vibration environments. By subjecting the product to increasing levels of stress, long term failure modes that would show up under normal operating conditions in months or years can be revealed in just hours or days.

An essential component of HALT is root cause analysis and the identification and implementation of corrective action to ensure the product integrity, thus increasing the product's reliability and the robustness of design.

Test Methodology

The process subjects the product to progressively higher stress levels, incorporating thermal dwells, rapid temperature transitions, vibration, and a combination of temperature and vibration to precipitate inherent defects. Moreover, HALT stresses the product to failure in order to assess design robustness and margin above its intended operation.

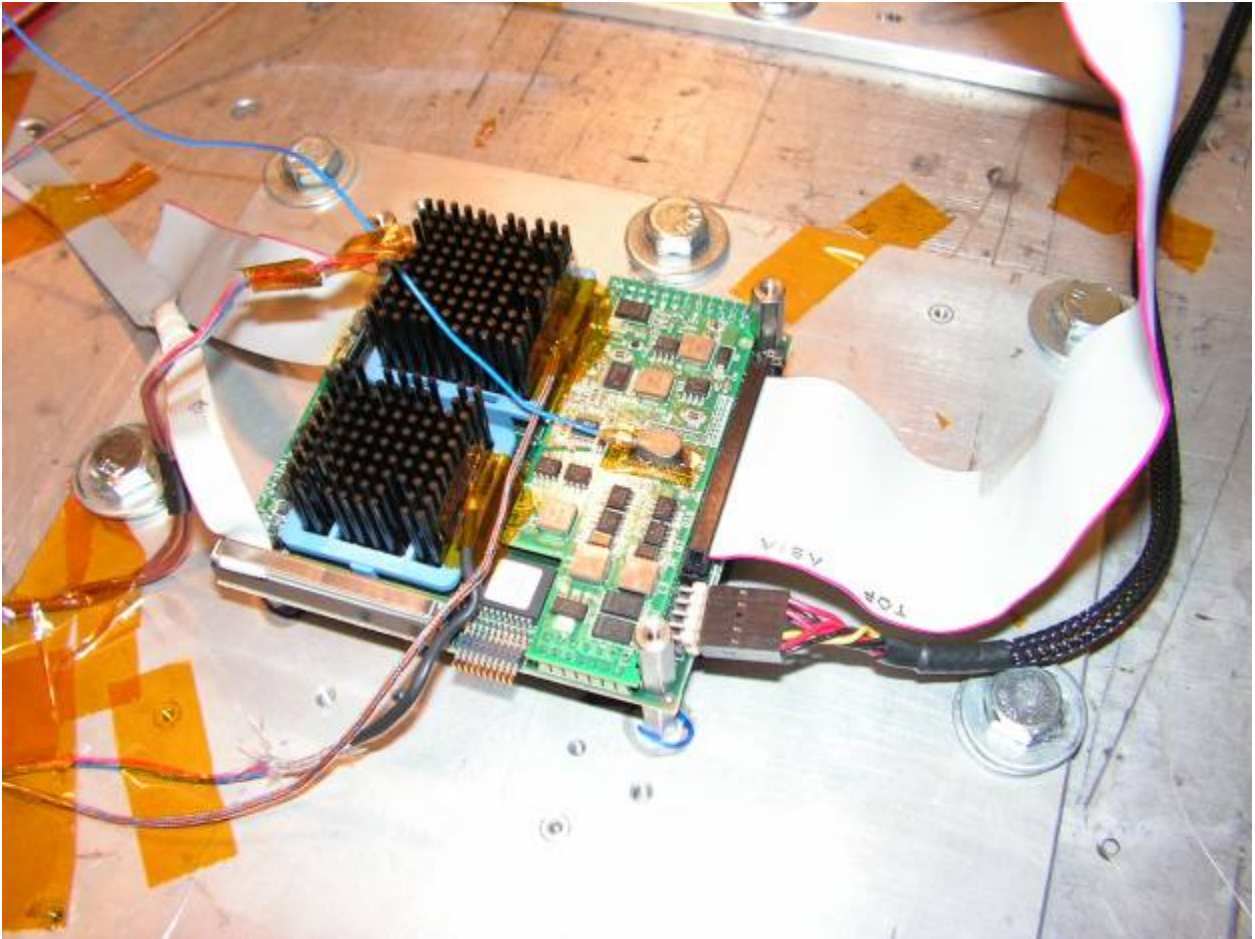


Figure 1. Test Setup

During the testing, the CoreModule 800 ran the following tests continuously, in order to exercise the entire circuit:

1	CPU 1Test	9	PCI Bus Test
2	NPU 1Test	10	APM Test
3	Test Timer	11	PCI Network Test
4	RTC Test	12	Com Port 1 Test
5	Interrupt Controller 1 Test	13	Com Port 2 Test
6	Interrupt Controller 2 Test	14	Base Memory Test
7	DMA Controller 1 Test	15	Extended Memory Test
8	DMA Controller 4 Test	16	Cache Memory Test

The CoreModule 800 was subjected to five tests: Cold Stress, Hot Stress, Rapid Thermal Transitions, Vibration Stress, and Combined Environment (temperature and vibration together).

Cold Stress

The cold temperature step stress began at +20°C and decreased in 10°C increments. The dwell time at each thermal step was 15 minutes. During the cold temperature step stress, a cover was placed over the CoreModule 800 to maintain the airflow below its specification limit. The limits were determined as follows.

Lower Operating Limit (LOL): <-60°C / -76°F

Lower Destruct Limit (LDL): <-60°C / -76°F

Hot Stress

The hot temperature step stress began at +30°C and increased in 10°C increments as shown in Figure 2. The dwell time at each thermal step was 15 minutes. The dwell time began after the chamber control thermocouples on the unit had stabilized. The results were as follows:

Upper Operating Limit (UOL): +90°C / +194°F

Upper Destruct Limit (UDL): >+100°C / +212°F

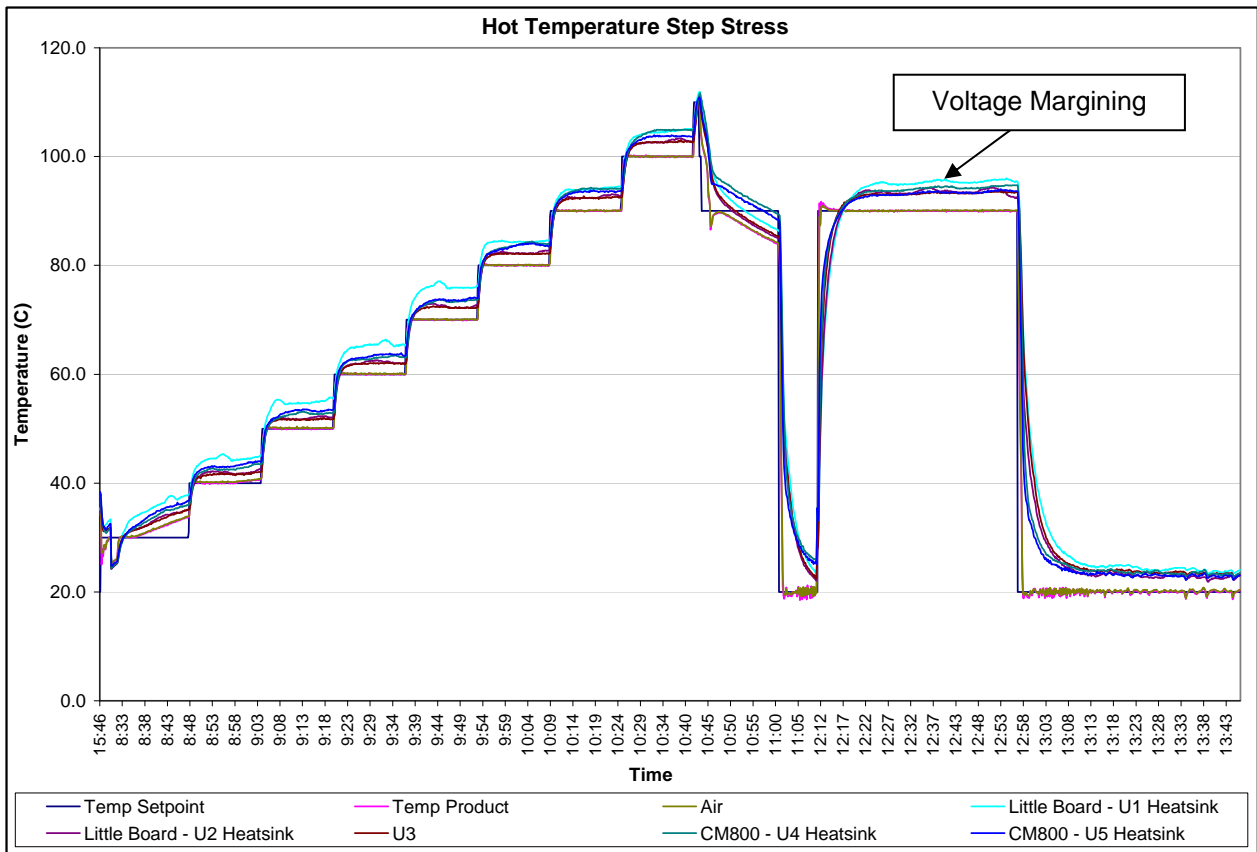


Figure 2. Hot Step Stress Plot

Rapid Thermal Transitions

CoreModule 800 was exposed to 5 rapid temperature cycles from -60°C to $+90^{\circ}\text{C}$ with a rate set to 60°C per minute. The measured and calculated results were:

Upper Set Point: $+90^{\circ}\text{C}$ / $+194^{\circ}\text{F}$

Lower Set Point: -60°C / -76°F

Calculated Chamber Air Rate of Change: 66°C / minute

Calculated Product Response Rate of Change: 61°C / minute

Vibration Stress

The product was mounted to the vibration table, and accelerometers were attached to measure the vibration response on the product..

The vibration step stress began at a set point of 5 Grms and was increased in 5 Grms increments. The dwell time at each set point was 15 minutes. After the 30 Grms level, the vibration was decreased to 5 Grms to determine if a failure occurred that was not detected at the higher vibration level. If a failure was not detected during this "tickle vibration", the vibration was increased to the next level. The temperature was set to 25°C .

Vibration levels were measured at two product locations during the vibration step stress. The vibration measurements on the product were taken using a National Instruments spectrum analyzer. The bandwidths used to calculate the Grms levels on the product were 2Hz to 2,500Hz and 2Hz to 10,000Hz using a digital filter at 2,500Hz and 10,000Hz. During each vibration step, a power spectral density plot was taken showing the calculated Grms level on the product and the distribution of energy over the desired frequency bands 2Hz to 2,500Hz and 2Hz to 10,000Hz.

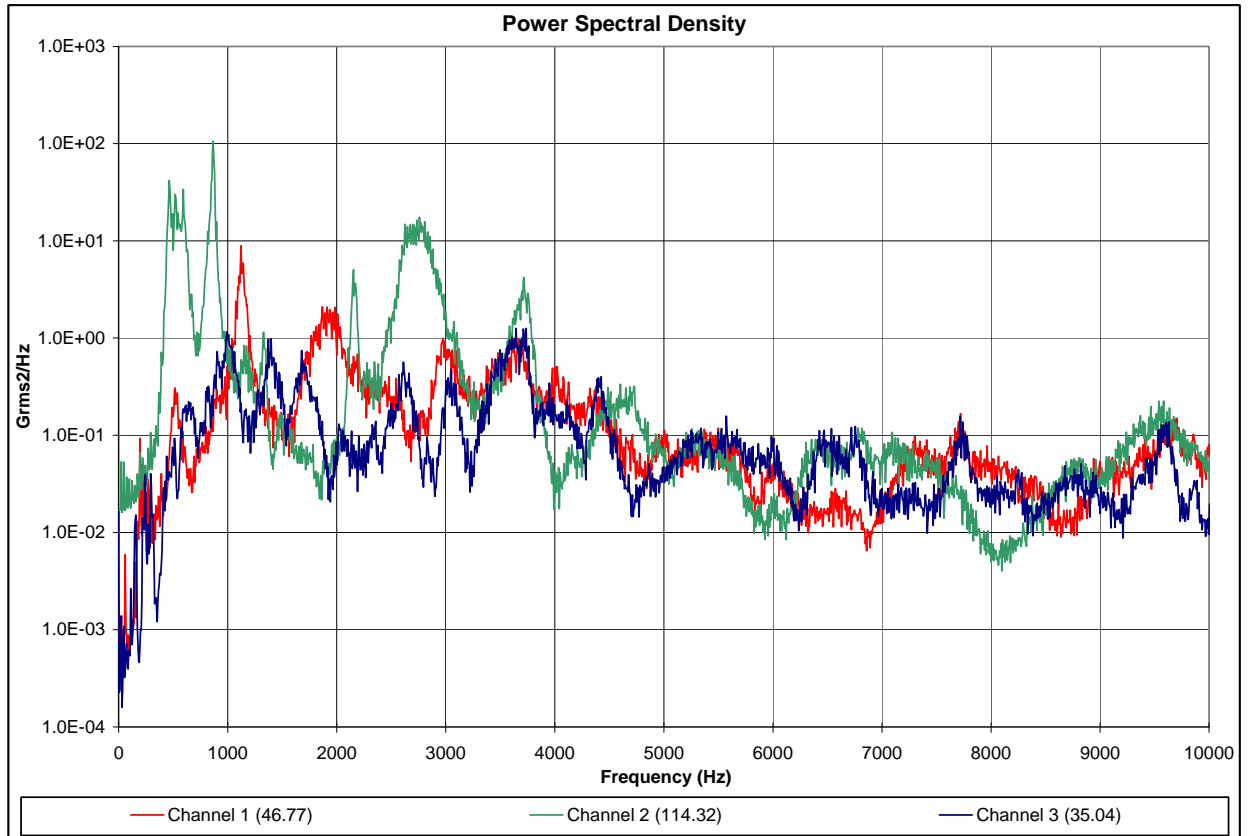


Figure 3. Vibration Plot: 50 Grms, from 2 Hz to 10 kHz

Combined Environment

The CoreModule 800 was exposed to 5 rapid temperature cycles from -60°C to +90°C combined with vibration, as shown in Figure 4. The vibration level was set to 6 Grms for the first temperature cycle and then increased in 6 Grms increments before each additional cycle.

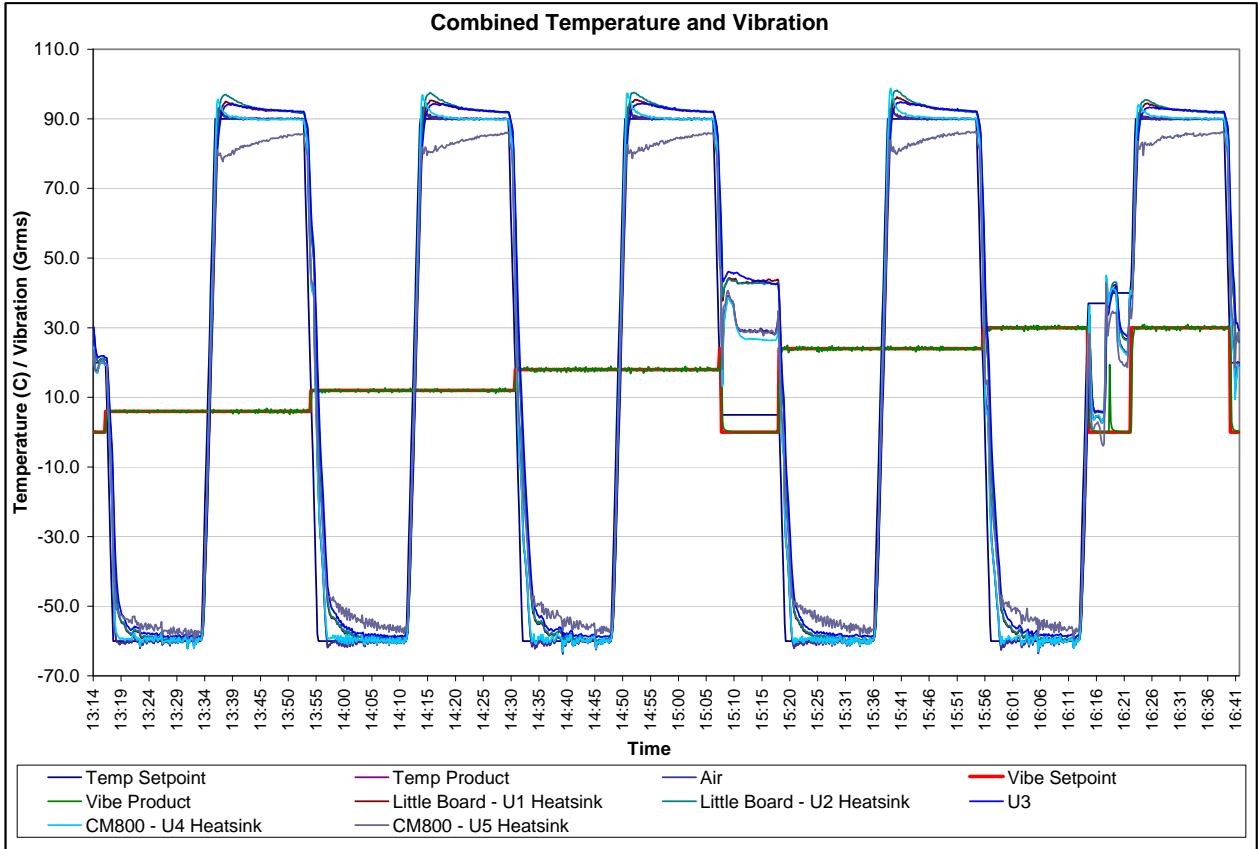


Figure 4. Combined Environment Plot

Table 1: Results: Operating Limit (OL) and Destruct Limit (DL)

Stress Condition	Chamber Setpoint
Cold Temperature OL	<-60°C (-76°F)
Hot Temperature OL	+90°C (+194°F)
Vibration OL	>50 Grms
Cold Temperature DL	<-60°C (-76°F)
Hot Temperature DL	>+100°C (+212°F)
Vibration DL	>50 Grms

Conclusion

The operating and destruct limits of the CoreModule 800 are shown in Table 1. This PCI-104 SBC has overcome strict design, manufacturing, and testing hurdles to prove suitability for extremely rugged applications.

*Link to CoreModule 800 Page: For more information on the CoreModule 800

*Link to the e-Store: To purchase this product

*Link to contact page: To contact your local representative, click here.