CoreModule™ 600
PC/104-Plus
Single Board Computer
Reference Manual

P/N 5001668A Revision A

Notice Page

NOTICE

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REVISION HISTORY

Revision	Reason for Change	Date
A	Initial Release	Jun/04

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Audience Assumptions

This reference manual is for the person who designs computer related equipment, including but not limited to hardware and software design and implementation of the same. Ampro Computers, Inc. assumes you are qualified in designing and implementing your hardware designs and its related software into your prototype computer equipment.

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the CoreModule™ 600 single board computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- CoreModule 600 SBC Specifications
- Environmental requirements
- Major chips and features implemented
- CoreModule 600 SBC connector/pin numbers and definition
- BIOS Setup information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

Reference Material

The following list of reference materials may be helpful for you to complete your custom design successfully. Most of this reference material is also available on the Ampro web site in the Embedded Design Resource Center. The Embedded Design Resource Center was created for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience.

Specifications

- PC/104 Specification, Revision 2.5, November, 2003
- PC/104-Plus Specification, Revision 2.0, November, 2003

  For latest revision of the PC/104 specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org
- PCI 2.2 Compliant Specifications, Revision 2.2, December 18, 1998

  For latest revision of the PCI specifications, contact the PCI Special Interest Group at:

  Web site: http://www.pcisig.com

Chip Specifications

The following integrated circuits (chips) are used in the CoreModule 600 single board computer:

- Intel Corporation and the ULV 400MHz Celeron® (0.13 µ) processor used for the embedded CPU

  Web site: http://www.intel.com
- VIA Technologies, Inc. and the chips, VT8606 and VT82C686B, used for the Northbridge/Video controller and Southbridge/Super I/O respectively.

  Web site: http://www.viatech.com

- Intel Corporation and the chip, 82551ER, used for the Ethernet controller

  Web site: http://developer.intel.com/design/network/products/82551er_DS

Related Ampro Products

The following items are directly related to successfully using the Ampro product you have just purchased or plan to purchase. Ampro highly recommends that you purchase and utilize a CoreModule 600 QuickStart Kit simultaneously with the design of your product.

CoreModule 600 Support Products

- CoreModule 600 QuickStart Kit (QSK)

  The CoreModule 600 QuickStart Kit includes the CoreModule 600 SBC, a complete cable kit with I/O Interface board, the CoreModule 600 QuickStart Guide, and drivers for Ampro supported operating systems with unique devices used on the board. The release notes, drivers, and documentation in PDF format are provided on the CoreModule 600 Documentation & Support Software CD-ROM.

- CoreModule 600 Development System

  The CoreModule 600 Development System is a benchtop system, which provides a "known good" environment for your development work. The Development System provides an integrated and easy-to-use self-hosted development environment that lets you maximize the benefit of using off-the-shelf PC-compatible modules as the basis of your embedded system design. You can install PC/104-Plus and PC/104 expansion modules or PCI and ISA bus expansion boards on the Development System chassis. The Development System is laid out to make all the components of your system accessible. Refer to the CoreModule 600 Development System Users Guide on the CoreModule 600 Documentation & Support Software CD-ROM for more information.

- CoreModule 600 Documentation & Support Software (Doc & SW) CD-ROM

  The CoreModule 600 Doc & SW CD-ROM is provided with the CoreModule 600 QuickStart Kit and Development System. The CD-ROM includes all of the CoreModule documentation in PDF format, including this reference manual, the CoreModule 600 QuickStart Guide, the CoreModule 600 Development System Users Guide, and software utilities and drivers.

Other CoreModule Products

- CoreModule™ 410 – This PC/104 embedded CPU is a state-of-the-art, high-integration x86-based computer using STMicroelectronics 133MHz STPC Elite processor, which provides a complete embedded PC solution with most of the standard peripheral interfaces. In addition to the standard CoreModule features (PC/104 form factor, PC/104 bus, +5 volt power, etc.), it includes 16MB soldered SDRAM memory, watchdog timer, serial console, BIOS extensions for OEM boot customization, and Advanced Power Management. The CoreModule 410 also offers a Bytewide socket supporting DiskOnChip 2000 devices and a GPIO interface for customer usage.

- CoreModule™ 420 – This embedded processor module is a state-of-the-art, high-integration x86-based computer on a single PC/104 board. The CoreModule 420, based on STMicroelectronics 133MHz STPC™ Atlas processor, provides a complete single board computer as an embedded PC solution with all of the standard peripheral interfaces. In addition to the standard CoreModule features (PC/104 form factor, PC/104 bus, +5 volt only power, etc.), it includes four serial ports, eight GPIOs, 64MB onboard SDRAM memory, Ethernet, USB, video for CRT and TFT flat panel support, watchdog timer, serial console, BIOS extensions for OEM boot customization, and Advanced Power Management. The CoreModule 420 also offers two types of solid-state disk interfaces, with a Bytewide socket supporting DiskOnChip 2000 devices as well as a Type II Socket supporting CompactFlash devices.

Other Ampro Products

- LittleBoard™ Family – These high-performance, rugged, highly integrated single-board computers use the EBX form factor (5.75x8.00 inches), and are available with Intel Pentium® III and Celeron® processors, as well as, other manufacturers processors. Check Ampro's web site for the most current processor support. The EBX-compliant LittleBoard single-board computers offer functions equivalent to a complete laptop or desktop PC system, plus several expansion cards. Most models feature dual Ethernet ports, high performance video, and PC/104-Plus expansion. Built-in extras to meet the critical requirements of embedded applications include onboard solid state disk capability, watchdog timer, smart power monitor, and other embedded-PC BIOS enhancements.
- ReadyBoard™ Family – These low-cost, high-performance single-board computers (SBC) use the EPIC form factor (4.5"x6.5") and are available with the VIA Eden™ processors, and Intel Pentium and Celeron processors. ReadyBoard products offer functions equivalent to a complete laptop or desktop PC system, plus several expansion cards. Ampro includes configuration control and embedded BIOS extension such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.
- MiniModule™ Family – This extensive line of peripheral interface modules, compliant with PC/104 and PC/104-Plus, can be used with Ampro's CoreModule, LittleBoard, and ReadyBoard single-board computers to complete the I/O requirements of embedded system solutions. Ampro's highly reliable MiniModule products currently support USB 2.0, IEEE 1394 (FireWire), CRT and flat-panel display interfaces, Ethernet, PC Card expansion, analog/data acquisition, FPGA, additional RS232/RS485 serial ports, and general-purpose I/O (GPIO).
- ETX Family – These high-performance, compact, rugged Computer-on-Module (COM) solutions use various x86 processors in an ETX Revision 2.6 form factor to plug into your custom baseboard. Each ETX module provides standard peripherals, including dual Ultra/DMA 33/66/100 IDE, floppy drive interface, PCI bus, ISA bus, serial, parallel, PS/2 keyboard and mouse interfaces, 10/100BaseT Ethernet, USB ports, Video, and AC'97 sound. ETX modules support up to 512MB of SODIMM DRAM. Unique to Ampro ETX COMs are a thicker PCB (50% thicker) and an optional temperature range, (–40°C to +85°C operation) to meet your rugged application requirements.
- EnCore™ Family – These high-performance, compact, rugged Computer-on-Module (COM) solutions use various processor technologies including Intel x86, MIPS®, and PowerPC™ architectures to plug into your custom logic board. Each EnCore module provides standard peripherals, including IDE, floppy drive interface, PCI bus, serial, parallel, PS/2 keyboard and mouse interfaces, 10/100BaseT Ethernet, and USB ports. Some EnCore modules also provide video and AC97 sound. Depending on the model, EnCore modules can hold between 16MB and 512MB of SODIMM SDRAM memory.

Chapter 2 Product Overview

This introduction presents general information about the PC/104 architecture and the CoreModule 600 single board computer (SBC). After reading this chapter you should understand:

- PC/104 concept
- CoreModule 600 architecture
- CoreModule 600 features
- Major components
- Connectors
- Specifications

PC/104 Architecture

The PC/104 architecture affords a great deal of flexibility in system design. You can build a simple system using only a CoreModule 600, input/output devices connected to the serial or parallel ports, and a CompactFlash card in the CompactFlash socket. To expand a simple CoreModule system, simply add self-stacking Ampro MiniModule expansion boards to provide additional capabilities, such as:

- Additional serial and parallel ports
- Analog or high-speed digital I/O
  - Data Acquisition (Analog In/Out)
  - USB 2.0 expansion modules
  - IEEE 1394 (FireWire) expansion modules
- PCMCIA interfaces
- FPGA (Field Programmable Gate Array) logic devices

PC/104 or PC/104-Plus expansion modules can be stacked with the CoreModule 600 avoiding the need for large, expensive card cages and backplanes. The PC/104-Plus expansion modules can be mounted directly to the PC/104 connectors of the CoreModule 600. PC/104-compliant modules can be stacked with an inter-board spacing of ~0.66 inches, so that, a 3-module system fits in a 3.6 inch by 3.8 inch by 2.4 inch space. See Figure 2-1.

One or more MiniModule products or other PC/104 modules can be installed on the CoreModule expansion connectors, so that the expansion modules fit within the CoreModule outline dimensions. Most MiniModule products have stackthrough connectors compatible with the PC/104-Plus Version 1.2 specification. Several modules can be stacked on the CoreModule headers. Each additional module increases the thickness of the package by ~17mm (0.66”). See Figure 2-1.

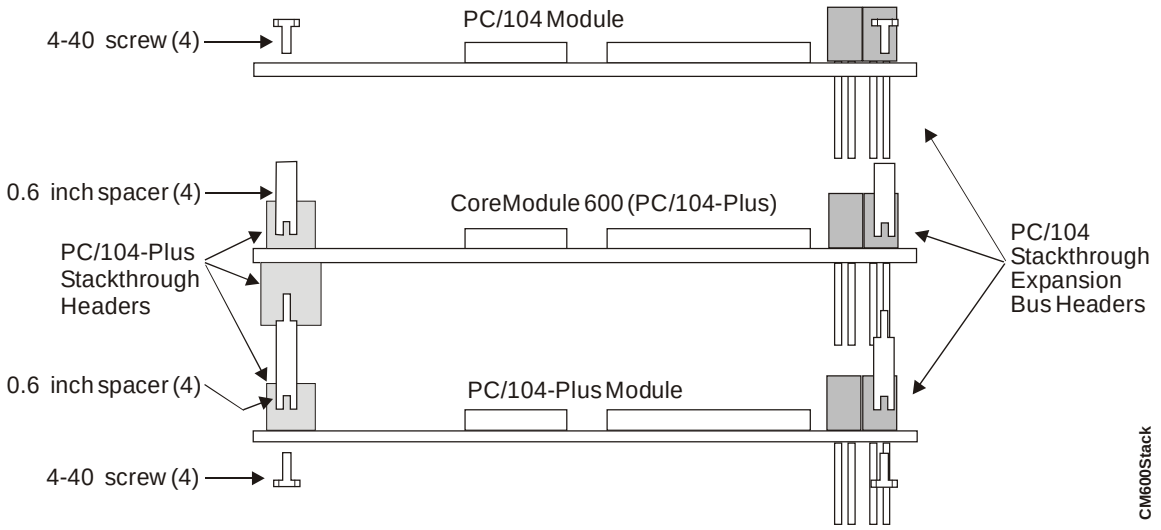

Figure 2-1. Stacking PC/104 Modules with the CoreModule 600

Product Description

The CoreModule 600 SBC is an exceptionally high integration, high performance, Ultra Low Voltage (ULV) Intel® Celeron processor based system compatible with the PC/104 standard. This rugged and high quality single-board system contains all the component subsystems of an ATX motherboard plus the equivalent of several PCI expansion boards.

The CoreModule 600 incorporates a VIA Technologies, Inc. Twister-T chipset and provides two serial ports, a EPP/ECP parallel port, two USB ports, PS/2 keyboard and mouse interfaces, floppy drive controller, one Ultra DMA 33/66/100 IDE controller supporting two IDE drives, and one 10/100BaseT Ethernet interface (external magnetics required). The CoreModule 600 also supports up to 256MB of onboard SDRAM memory and a AGP4x graphics controller, included in the Northbridge chip, which provides CRT and flat panel video interfaces for most popular LCD panels. .

The CoreModule 600 can be expanded through the PC/104 and PC/104-Plus expansion buses for additional system functions. These busses offer compact, self-stacking, modular expandability. The PC/104 is an embedded system version of the signal set provided on a desktop PC's ISA bus. The PC/104-Plus bus includes this signal set, and in addition, signals implementing a PCI bus, available on an additional 120-pin (4 rows of 30 pins) PCI expansion bus connector. The onboard Ethernet is internally connected to its PCI bus. This PCI bus operates at clock speeds up to 33MHz.

The CoreModule 600 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with Ampro MiniModules™ or other PC/104-compliant expansion modules, or it can be used as a powerful computing engine. The CoreModule 600 requires a single +5V power source.

Module Features

- CPU features
  - Ultra Low Voltage Intel 400MHz Celeron processor
  - Front Side Bus (FSB) speed of 100MHz
  - 256kB L2 Cache on the chip

- Memory
  - 256MB standard SDRAM soldered on the board
  - 100MHz Clock Speed
  - 512kB boot block Flash device
- Interface Buses
  - PC/104 and PC/104-Plus Bus Interfaces
  - PC/104 Bus speeds up to 8MHz (16-bit ISA Bus)
  - PC/104-Plus Bus speed at 33MHz (32-bit PCI Bus)
  - PCI 2.2 compliant
- IDE Interface
  - Supports two enhanced IDE devices
  - Supports single master mode
  - Supports Ultra DMA 100/66/33 in master mode
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
- CompactFlash Adapter Socket
  - Supports Type I or Type II PC cards
  - Supports IDE CompactFlash card
  - Supports bootable CompactFlash card
  - Supports primary IDE with Master/Slave jumper
  - Supports +3.3V or +5V PC cards (voltage selection jumper)
- Utility Interface
  - Floppy Disk Interface
    - Supports one floppy drive (Shared with Parallel Port)
    - Supports all standard PC/AT formats: 360kB, 1.2MB, 720kB, 1.44MB, 2.88MB
  - Parallel Port Interface
    - Supports standard printer port (Shared with Floppy Disk Drive Port)
    - Supports IEEE standard 1284 protocols, and EPP, ECP outputs
    - Bi-directional data lines
    - Supports 16 byte FIFO for ECP mode.
  - Serial Port Interface
    - Supports two RS232 serial ports with full handshaking
    - Port 1 supports full modem capability and RS485
    - Provides 16550-equivalent controllers
    - Supports two 16-byte FIFO buffer
    - Supports programmable word length, stop bits, and parity
    - Supports 16-bit programmable baud-rate generator
    - Supports an interrupt generator

- USB Port Interface
  - Supports one root USB hub
  - Supports two USB ports
  - Supports USB V1.1 and Universal OHCI v1.1
- PS/2 Keyboard and PS/2 Mouse Interface
- Supports external battery for Real Time Clock operation
- Supports standard PC speaker port with 0.1 watt output drive
- Supports a Reset switch for system reset

- Ethernet Interface
  - Intel 82551ER Controller chip
  - Supports on Ethernet port
  - Supports IEEE 802.3 10BaseT/100BaseTX compatible physical layer
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full duplex mode
    - Half-duplex mode supports enhance proprietary collision reduction mode
  - Requires an external isolation transformer
- Video Interfaces (CRT/LCD)
  - Support CRT (1600 x 1200 x 24) with 32MB SMA (Shared Memory Area)
  - AGP 4X graphics
  - Compliant with Rev 2.0 of AGP Interface
  - 24-bit flat panel outputs (LCD/TFT)
- Miscellaneous
  - Real-time clock (RTC) with external replaceable battery
  - Battery-less boot
  - Oops! Jumper support
  - Serial Console support
  - Watchdog Timer
  - Splash Screen

Block Diagram

Figure 2-3 shows the functional components of the module.

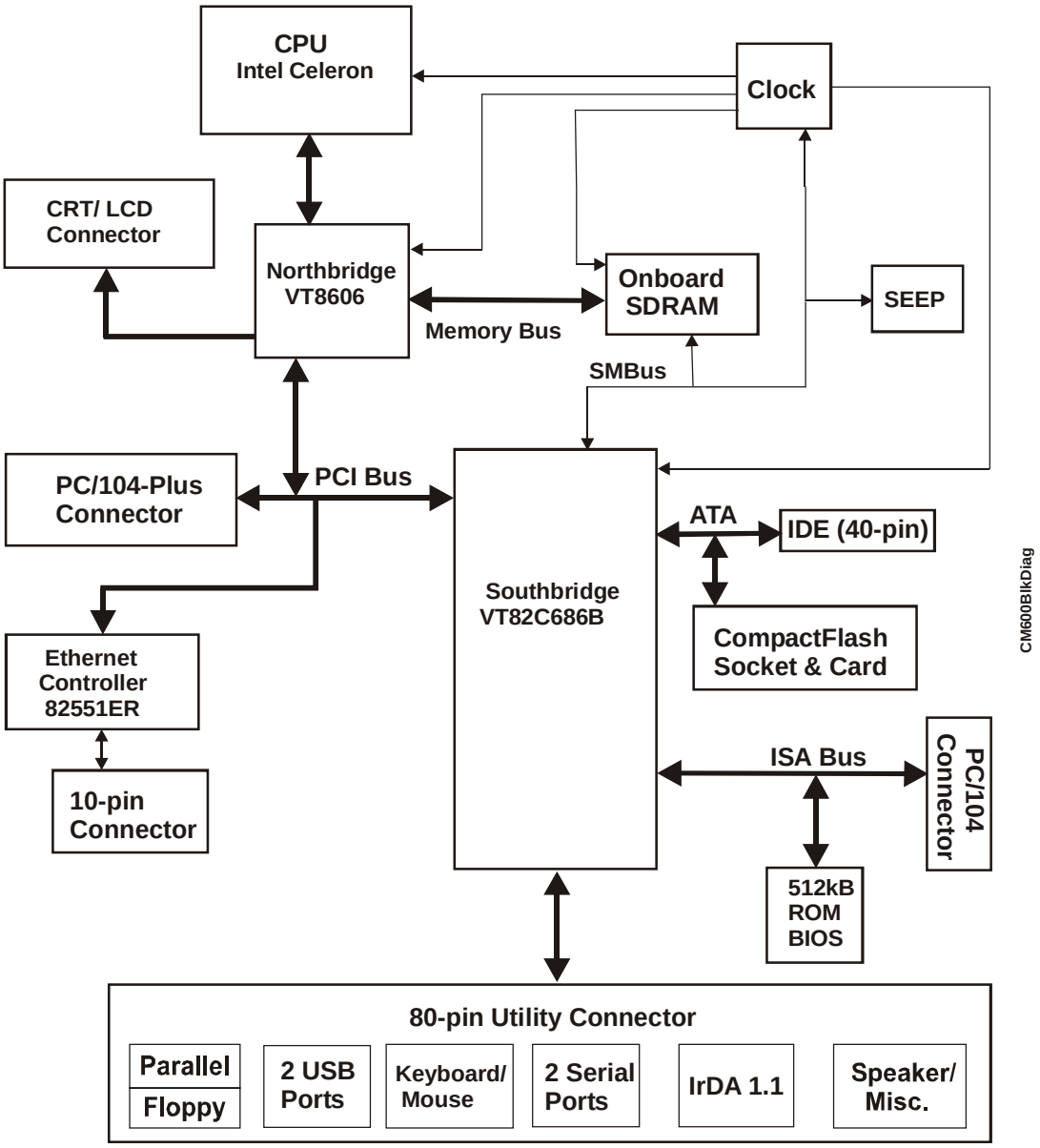

Figure 2-2. CoreModule 600 Block Diagram

Major Integrated Circuits (ICs)

Table 2-1 lists the major integrated circuits, including a brief description of each, on the CoreModule 600. Figures 2-3 and 2-5 show the locations of the major chips.

Table 2-1. Major Integrated Circuit Descriptions and Function

Chip Type	Mfg.	Model	Description	Function
CPU (U22)	Intel	Celeron (ULV)	400MHz processor	Embedded CPU
Northbridge and Video controller (U6)	VIA Technologies	VT8606	Northbridge functions plus Video	Memory and Video
Southbridge and Super I/O Controller (U12) (See Figure 2-5)	VIA Technologies	VT82C686B	Integrated Southbridge and Super I/O controller contains the floppy, parallel, serial, IDE, infrared (IrDA), speaker, keyboard/mouse, and USB controllers.	I/O functions
Ethernet Controller (U7)	Intel	82551ER	Ethernet Controller – This chip provides the 10/100BaseT Ethernet function.	Ethernet

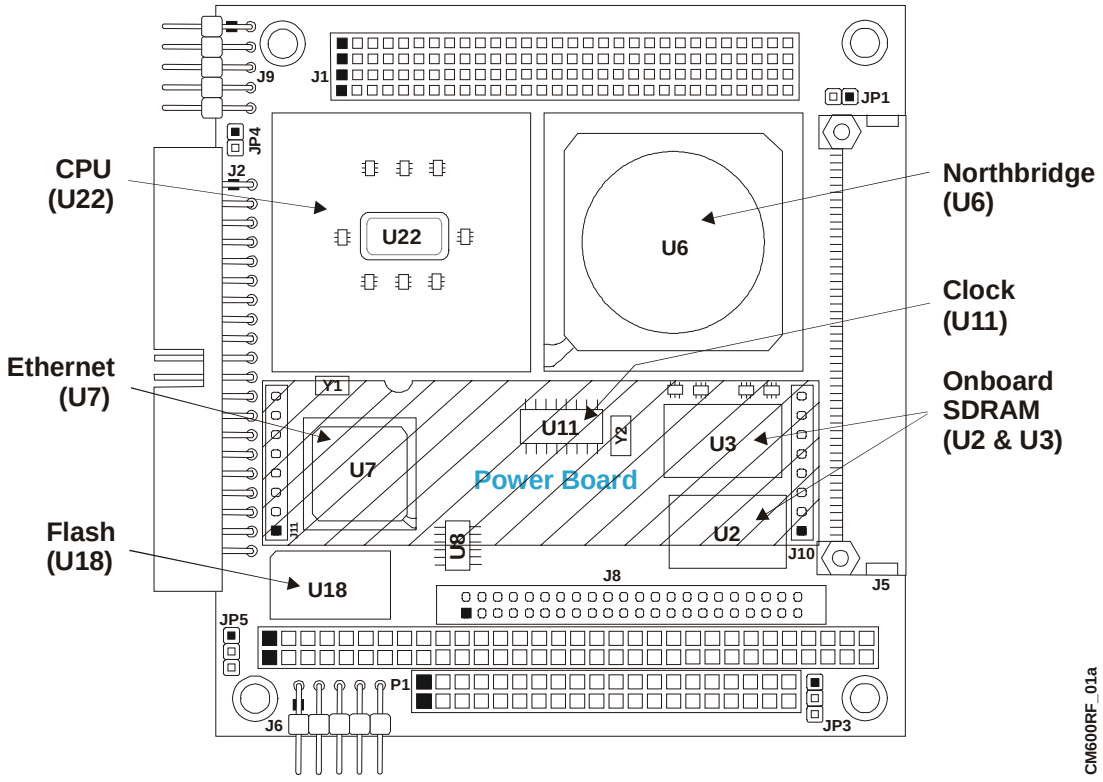

Figure 2-3. Component Locations (Top view)

Connectors and Jumpers

Connector Definitions

Table 2-2 describes the connectors shown in Figures 2-4 to 2-5. All connectors use 0.1" pin spacing unless otherwise indicated.

Table 2-2. Module Connector Descriptions

Jack/Plug #	Board Access	Description
P1 A, B, C, D – PC/104	Top/ Bottom	104-pin connector used for PC/104 signals
J1 – PC/104-Plus	Top/ Bottom	120-pin connector used for PC/104-Plus signals
J2 – IDE	Top	40-pin connector used for the IDE devices
J3 – CompactFlash	Bottom	50-pin socket used for CompactFlash cards
J5 – Utility	Top	80-pin connector used for most I/O functions
J6 – Power	Top	10-pin connector used for external Power connection
J8 – Video	Top	44-pin connector used for the CRT/LCD interface
J9 – Ethernet	Top	8-pin connector used for the Ethernet interface
J10 – On board PWR	Top	10-pin connector used for daughter power board
J11 – On board PWR	Top	10-pin connector used for daughter power board

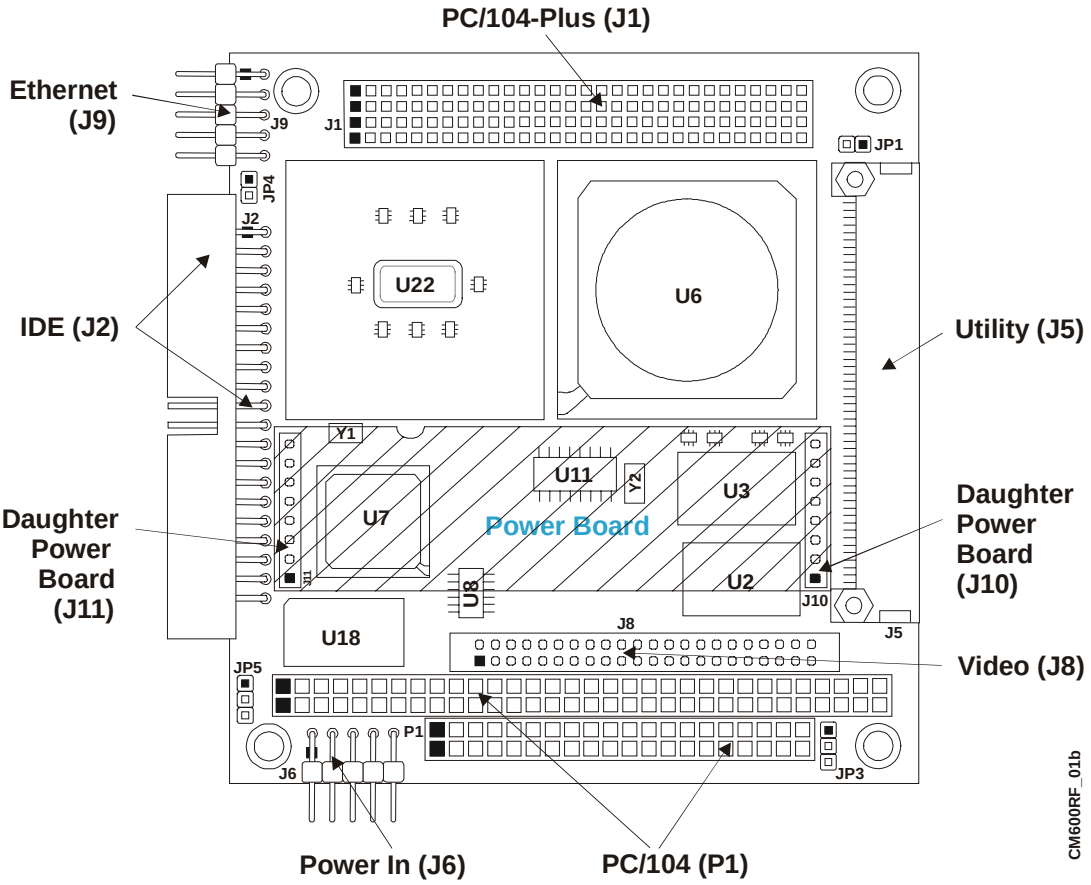

Figure 2-4. Connector Locations (Top view)

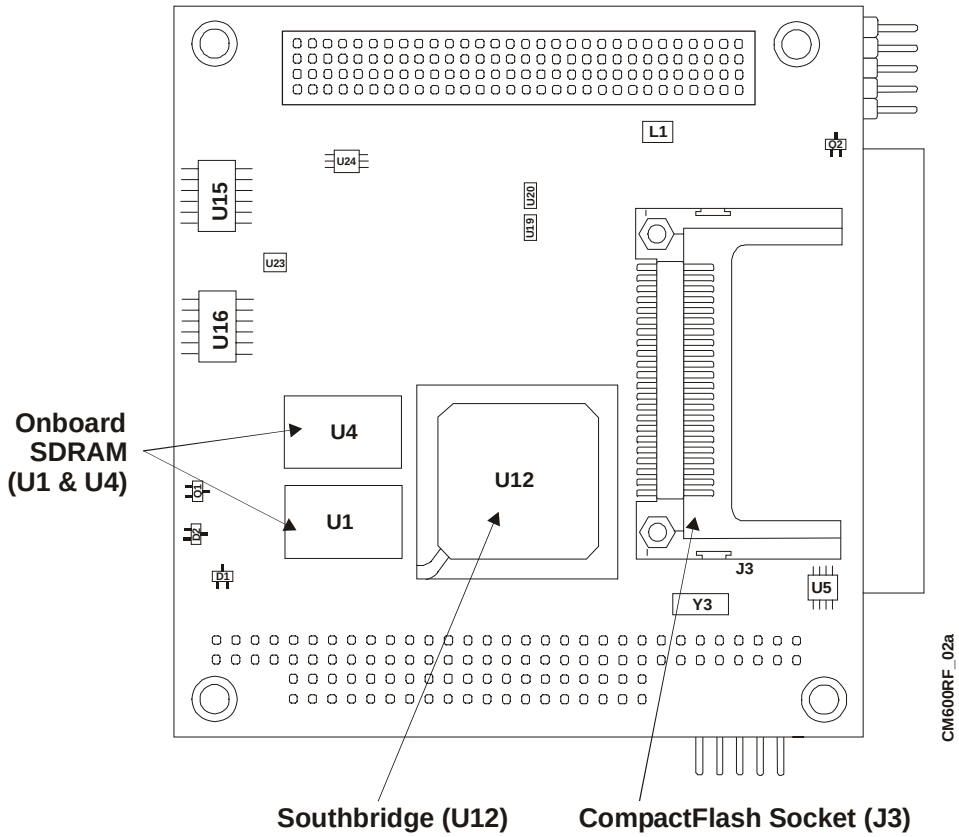

Figure 2-5. Components and Connector Locations (Bottom view)

Jumper Definitions

Table 2-3 describes the jumpers shown in Figure 2-6.

Table 2-3. Jumper Settings

Jumper #	Installed	Removed/Enabled
JP1 – Serial 1 RS485 Termination	Enable Termination (1-2) **(Default)**	Disable Termination (Removed)
JP3 – Flat Panel Voltage Selection	Enable +3.3V (1-2) **(Default)**	Enable +5V (2-3)
JP4 – CompactFlash Master/Slave	Enable Master (pins 1-2)	Enable Slave (Removed) **(Default)**
JP5 – CompactFlash Voltage Selection	Enable +5V (1-2)	Enable +3.3V (2-3) **(Default)**

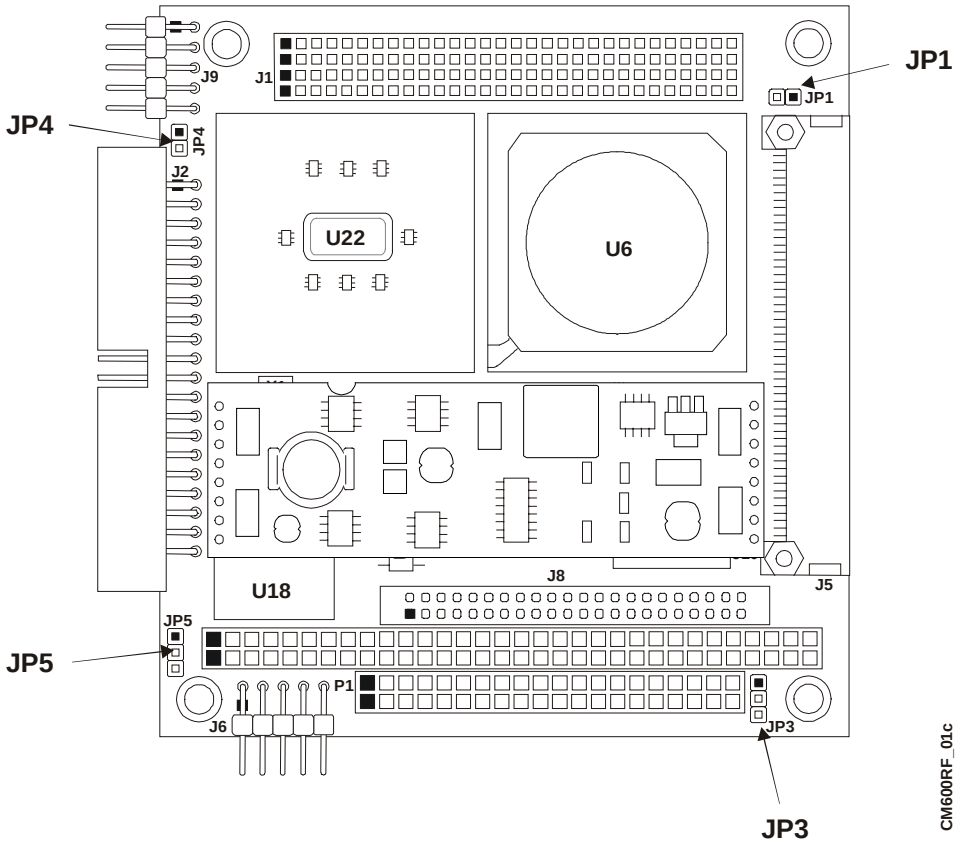

Figure 2-6. Jumper Locations (Top view)

Specifications

Physical Specifications

Table 2-4 gives the physical dimensions of the module and Figure 2-7 gives the mounting dimensions.

Table 2-4. Weight and Footprint Dimensions

Item	Dimension
Weight	0.108kg. (0.238lbs.)
Height (overall)	10.668 mm (0.420 inches)
Board thickness	2.362 mm (0.093 inches)
Width	90.2 mm (3.6 inches)
Length	95.9 mm (3.8 inches)

NOTE Overall height is measured from the upper board surface to the highest permanent component (PC/104 bus connector) on the upper board surface. This measurement does not include the heatsink, which can vary. The heatsink could increase this dimension.

Mechanical Specifications

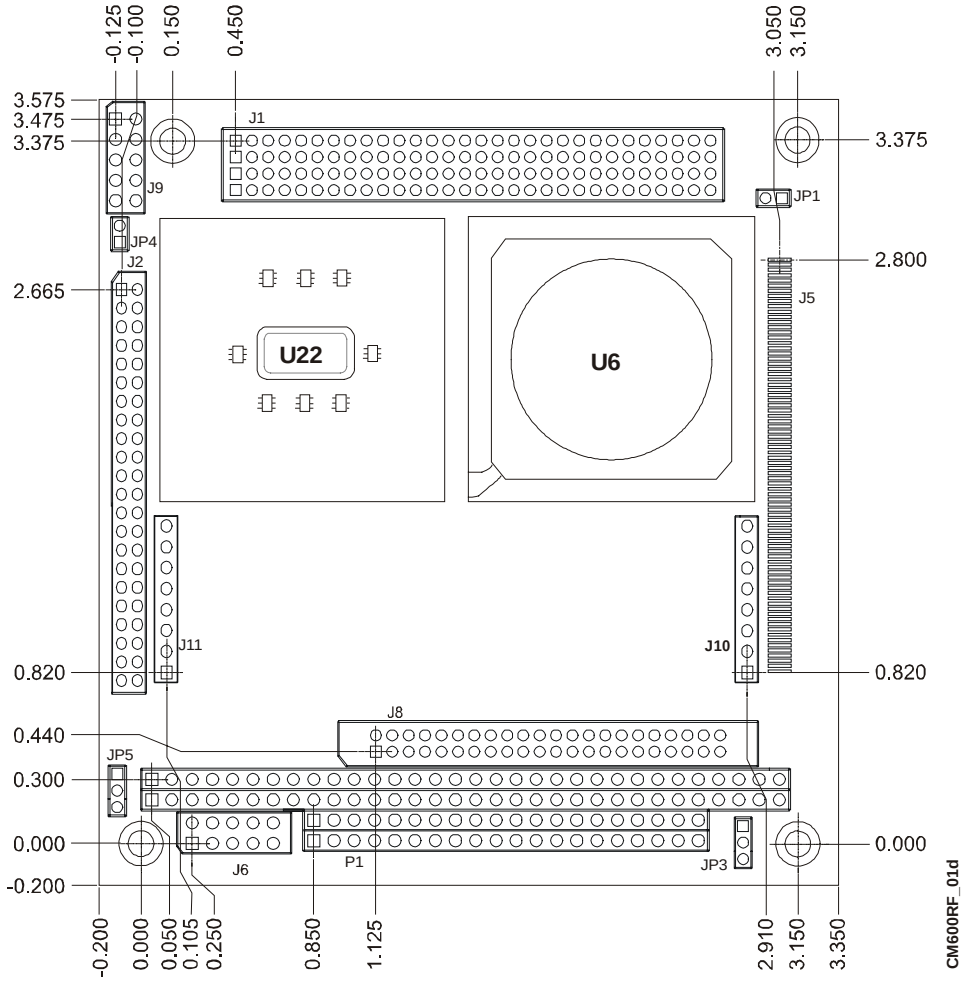

Figure 2-7. Mechanical Dimensions (Top View)

NOTE All dimensions are given in inches. Pin 1 is shown as a black square in jumpers and connectors in all illustrations.

Power Specifications

Table 2-5 shows the power requirements.

Table 2-5. Power Supply Requirements

Parameter	400MHz Characteristics
Input Type	Regulated DC voltage
In-rush Voltage & Current	+5 VDC +/- 5% @ 2.34 Amps
BIT* Voltage & Current	+5 VDC +/- 5% @ 1.84 Amps
Typical Operating Power	9.20W

Operating conditions: The InRush value has only video, 128MB PC/100 RAM, and power connected.

*BIT = Burn-In-Test value has the following devices and memory connected, including input power: CRT video, 128MB PC/100 RAM, hard disk drive, floppy, I/O Interface board, keyboard, mouse, serial ports with loopbacks, USB with loopbacks, and the Ethernet port connected operating under MS Windows 2000.

Environmental Specifications

Table 2-6 provides the most efficient operating and storage condition ranges required for this module.

Table 2-6. Environmental Requirements

Parameter	Conditions
Temperature	
Operating	+0° to +70° C (32° to 158° F)
Extended (Optional)	–40° to +85° C (–40°F to +185°F)
Storage	–55° to +85° C (–67°F to +185°F)
Humidity	
Operating	20% to 80% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU, Northbridge, Southbridge, and the voltage regulators are the primary sources of heat generated on the board. The CoreModule 600 ships from the factory with a heatsink installed on the CPU, but may not be shown in all illustrations for simplicity.

Chapter 3 Hardware

Overview

This chapter discusses the chips and connectors of the module features in the following order:

- CPU (U22)
- Memory
  - Onboard SDRAM (U1, U2, U3, U4)
  - Flash Memory (U18)
- PC/104-Plus Bus (J1)
- PC/104 Bus (P1A, B, C, D)
- IDE (J2)
- CompactFlash Socket (J3)
- Utility (J5)
  - Floppy Interface
  - Serial Interface
  - Parallel Interface
  - USB Interface
  - Infrared (IR) Interface
  - Keyboard
  - Mouse
  - External Battery
  - Reset Switch
  - Speaker
- Ethernet (J9)
- Video (J8)
- Miscellaneous
  - Time of Day/RTC
  - Oops! Jumper
  - Serial Console
  - Watchdog timer
- Power (J6)

NOTE	Ampro Computers, Inc. only supports the features/options tested and listed in this manual. The main chips used in the CoreModule 600 may provide more features or options than are listed for the CoreModule 600, but some of these features/ options are not supported on the module and will not function as specified in the chip documentation.

CPU (U22)

The CoreModule 600 uses the Ultra Low Voltage (ULV) Intel® Celeron® processor as the embedded processor. This ULV Celeron (0.13µ) processor in the Micro FC-BGA package is a high-performance Intel processor at 400MHz with 256kB L2 Cache on chip operating at 100MHz FSB (front side bus). The ULV Celeron processor requires a heatsink, but no fan.

Memory

The CoreModule 600 consists of the following memory elements:

- SDRAM chips (4x)
- Flash memory

Onboard SDRAM Memory (U1, U2, U3, U4))

The CoreModule 600 contains four 16-bit SDRAM chips supporting 256MB of memory soldered into place on the module and operating at 100MHz.

Flash Memory (U18)

There is an 8-bit wide, 512kB flash device used for system BIOS and is connected to the Southbridge, VT82C686B, through an ISA bus transceiver. The BIOS is re-programmable and the features supported are detailed in Chapter 4, *BIOS Setup*.

Memory Map

Table 3-1. Memory Map

Base Address	Function
00000000h - 0009FFFFh	Conventional Memory
000A0000h - 000AFFFFh	Graphics Memory
000B0000h - 000B7FFFh	Mono Text Memory
000B8000h - 000BFFFFh	Color Text Memory
000C0000h - 000C7FFFh	Standard Video BIOS
000F0000h - 000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
00100000h - 04000000h	Extended Memory (If onboard VGA is enabled, then the amount of memory assigned is subtracted from extended memory)
FFF80000h - FFFFFFFFh	System Flash

Interrupt Channel Assignments

The channel interrupt assignments are shown in Table 3-2.

Table 3-2. Interrupt Channel Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Keyboard		X														
Secondary Cascade			X													
COM1					D											
COM2				D	O											
Floppy							X									
Parallel						O		D								
RTC									X							
IDE Primary															X	O
Math Coprocessor														X		
PS/2 Mouse													X			
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
USB	Automatically Assigned															
VGA	Automatically Assigned															
Ethernet	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed

NOTE	The IRQs for the Ethernet, Video, and Internal Local Bus (ISA) are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

I/O Address Map

Table 3-3 shows the I/O address map.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
0000-000F	Primary DMA Controller (#1)
0020-0021	Master Interrupt Controller (#1)
0040-0043	Programmable Interrupt Timer (Clock/Timer)
0060	Keyboard Controller
0061	ISA Standard Port B
0063	ISA Standard Port B alias
0064	Keyboard Controller
0065	ISA Standard Port B alias
0067	ISA Standard Port B alias
0069	ISA Standard Port B alias
006B	ISA Standard Port B alias
006D	ISA Standard Port B alias
006F	ISA Standard Port B alias
0070-0071	RTC/ NMI enable
0080-008F	DMA Page
00A0-00A1	Slave Interrupt Controller (#2)
00C0-00DF	Secondary DMA Controller (#2)
01F0-01F7	IDE 0 (can be disabled)
0201	Watchdog trigger (disabled by default)
02F8-02FF	Serial Port 2 (COM2) (base configuration @ 3F8h/**2F8h**/3E8h/2E8h/7F8h/7E8h/disabled)
0370-0371	Super I/O Configuration
0378-037B	LPT 1 (base configuration @ 378h/278h/3BCh/disabled; (3BCh does not support EPP mode)
0378-037F	LPT 1 (only in EPP modes, with default base address)
03F0-03F5	Floppy Disk Controller (can be disabled)
03F6	IDE 0 (see 1F0)
03F7	Floppy Disk Controller (see 3F0)
03F8-03FF	Serial Port 1 (COM1) (base configuration @ **3F8h**/2F8h/3E8h/2E8h/7F8h/ 7E8h/disabled)
0778-077A	LPT 1 (only in ECP modes, with default base address)
0CF8	PCI Configuration Address
0CFC-0CFF	PCI Configuration Data
E000-E007	General Purpose I/O for customer use
E400-E407	Board control
E800-E80F	IDE Bus Master registers
EC00	IDE 1 Control (IDE 1 not routed to a connector)
F000-F007	IDE 1 Command (IDE 1 not routed to a connector)

PC/104-Plus Interface (J1)

The PC/104-Plus uses a 120-pin (30x4) header interface. This interface header will carry all of the appropriate PCI signals operating at clock speeds up to 33MHz. The Northbridge, VT8606, integrates a PCI arbiter that supports up to four devices with three external PCI masters. This interface header is stackable and is located both on the top and bottom of the board.

Table 3-4 provides the signals and descriptions for each of the PC/104-Plus bus pin-outs.

Table 3-4. PC/104-Plus Pin/Signal Descriptions (J1)

Pin #	Signal	Input/ Output	Description
1 (A1)	GND/ (Key)		Key – Digital Ground
2 (A2)	VI/O		+5 volts ±5% power supply
3 (A3)	AD05	T/S	Address and Data Bus Line 5 – There are 32 multiplexed signal lines (address and data). A bus transaction consists of an address followed by one or more data cycles.
4 (A4)	C/BE0*	T/S	Bus Command/Byte Enable 0 – This signal is one of four multiplexed signal lines. During the address cycle, the command is defined and during the data cycle, the byte enable is defined.
5 (A5)	GND		Digital Ground
6 (A6)	AD11	T/S	Address and Data Bus Line 11 – Refer to Pin 3 for more information.
7 (A7)	AD14	T/S	Address and Data Bus Line 14 – Refer to Pin 3 for more information.
8 (A8)	+3.3V		+3.3 volts ±5% power supply
9 (A9)	SERR*	O/D	System Error – This signal is for reporting address parity errors.
10 (A10)	GND		Digital Ground
11 (A11)	STOP*	S/T/S	Stop – This signal indicates the current selected device is requesting the master to stop the current transaction
12 (A12)	+3.3V		+3.3 volts ±5% power supply
13 (A13)	FRAME*	S/T/S	Frame Access – This signal is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle.
14 (A14)	GND		Digital Ground
15 (A15)	AD18	T/S	Address and Data Bus Line 18 – Refer to Pin 3 for more information.
16 (A16)	AD21	T/S	Address and Data Bus Line 21 – Refer to Pin 3 for more information.
17 (A17)	+3.3V		+3.3 volts ±5% power supply
18 (A18)	IDSEL0	In	Initialization Device Select 0 – This signal is one of four signal lines used as the chip-select signals during configuration.
19 (A19)	AD24	T/S	Address and Data Bus Line 24 – Refer to Pin 3 for more information.
20 (A20)	GND		Digital Ground
21 (A21)	AD29	T/S	Address and Data Bus Line 29 – Refer to Pin 3 for more information.
22 (A22)	+5V		+5 volts ±5% power supply
23 (A23)	REQ0*	T/S	Bus Request 0 – This signal is one of three signal lines that indicate to the arbitrator when the device desires use of the bus.
24 (A24)	GND		Digital Ground

Pin #	Signal	Input/ Output	Description
25 (A25)	GNT1*	T/S	Grant 1 – This signal is one of three signal lines that indicate access has been granted to the requesting device (PCI Masters).
26 (A26)	+5V		+5 volts ±5% power supply
27 (A27)	CLK2	In	PCI clock 2 – This signal is one of four signal lines, that provide timing outputs for four external PCI devices and timing for all transactions on the PCI bus.
28 (A28)	GND		Digital Ground
29 (A29)	+12V		+12 volts ±5% power supply
30 (A30)	NC		Not connected - Reserved
31 (B1)	NC		Not connected - Reserved
32 (B2)	AD02	T/S	Address and Data Bus Line 2 – Refer to Pin 3 for more information.
33 (B3)	GND		Digital Ground
34 (B4)	AD07	T/S	Address and Data Bus Line 7 – Refer to Pin 3 for more information.
35 (B5)	AD09	T/S	Address and Data Bus Line 9 – Refer to Pin 3 for more information.
36 (B6)	VI/O		+5 volts ±5% power supply
37 (B7)	AD13	T/S	Address and Data Bus Lines 13 – Refer to Pin 3 for more information.
38 (B8)	C/BE1*	T/S	Bus Command/Byte Enable 1 – Refer to Pin 4 for more information.
39 (B9)	GND		Digital Ground
40 (B10)	PERR*		Parity Error – This signal is for reporting data parity errors.
41 (B11)	+3.3V		+3.3 volts ±5% power supply
42 (B12)	TRDY*	S/T/S	Target Ready – This signal indicates the selected device's ability to complete the current transaction cycle. Both IRDY* and TRDY* must be asserted to terminate a data cycle.
43 (B13)	GND		Digital Ground
44 (B14)	AD16	T/S	Address and Data Bus Line 16 – Refer to Pin 3 for more information.
45 (B15)	+3.3V		+3.3 volts ±5% power supply
46 (B16)	AD20	T/S	Address and Data Bus Lines 20 – Refer to Pin 3 for more information.
47 (B17)	AD23	T/S	Address and Data Bus Line 23 – Refer to Pin 3 for more information.
48 (B18)	GND		Digital Ground
49 (B19)	C/BE3*	T/S	Bus Command/Byte Enable 3 – Refer to Pin 4 for more information.
50 (B20)	AD26	T/S	Address and Data Bus Line 26 – Refer to Pin 3 for more information.
51 (B21)	+5V		+5 volts ±5% power supply
52 (B22)	AD30	T/S	Address and Data Bus Line 30 – Refer to Pin 3 for more information.
53 (B23)	GND		Digital Ground
54 (B24)	REQ2*	T/S	Bus Request 2 – Refer to pin 23 for more information.
55 (B25)	VI/O		+5 volts ±5% power supply
56 (B26)	CLK0	In	PCI clock 0– Refer to Pin 27 for more information
57 (B27)	+5V		+5 volts ±5% power supply

Pin #	Signal	Input/ Output	Description
58 (B28)	INTD*	O/D	Interrupt D – This signal only request interrupts for multi-function devices.
59 (B29)	INTA*	O/D	Interrupt A – This signal is used to request an interrupt.
60 (B30)	REQ3*	T/S	Bus Request 3 – Refer to Pin A23 for more information.
61 (C1)	+5		+5 volts ±5% power supply
62 (C2)	AD01	T/S	Address and Data Bus Line 1 – Refer to Pin 3 for more information.
63 (C3)	AD04	T/S	Address and Data Bus Line 4 – Refer to Pin 3 for more information.
64 (C4)	GND		Digital Ground
65 (C5)	AD08	T/S	Address and Data Bus Line 8 – Refer to Pin 3 for more information.
66 (C6)	AD10	T/S	Address and Data Bus Line 10 – Refer to Pin 3 for more information.
67 (C7)	GND		Digital Ground
68 (C8)	AD15	T/S	Address and Data Bus Line 15 – Refer to Pin 3 for more information.
69 (C9)	SB0*		Snoop Back Off – Not used (10k Pull-up resistor to 3.3V)
70 (C10)	+3.3V		+3.3 volts ±5% power supply
71 (C11)	LOCK*	S/T/S	Lock – This signal indicates an operation that may require multiple transactions to complete
72 (C12)	GND		Digital Ground
73 (C13)	IRDY*	S/T/S	Initiator Ready – This signal indicates the master's ability to complete the current transaction data cycle.
74 (C14)	+3.3V		+3.3 volts ±5% power supply
75 (C15)	AD17	T/S	Address and Data Bus Line 17 – Refer to Pin 3 for more information.
76 (C16)	GND		Digital Ground
77 (C17)	AD22	T/S	Address and Data Bus Line 22 – Refer to Pin 3 for more information.
78 (C18)	IDSEL1		Initialization Device Select 1 – Refer to Pin 18 for more information
79 (C19)	VI/O		+5 volts ±5% power supply
80 (C20)	AD25	T/S	Address and Data Bus Line 25 – Refer to Pin 3 for more information.
81 (C21)	AD28	T/S	Address and Data Bus Line 28 – Refer to Pin 3 for more information.
82 (C22)	GND		Digital Ground
83 (C23)	REQ1*	T/S	Bus Request 1 – Refer to Pin 23 for more information.
84 (C24)	+5V		+5 volts ±5% power supply
85 (C25)	GNT2*	T/S	Grant 2 – Refer to Pin 25 for more information
86 (C26)	GND		Digital Ground
87 (C27)	CLK3	In	PCI clock 3 – Refer to Pin 27 for more information
88 (C28)	+5V		+5 volts ±5% power supply
89 (C29)	INTB*	O/D	Interrupt B – This signal only request interrupts for multi-function devices.
90 (C30)	GNT3*	T/S	Grant 3 – Refer to Pin A25 for more information.
91 (D1)	AD00	T/S	Address and Data Bus Line 0 – Refer to Pin 3 for more information.
92 (D2)	+5V		+5 volts ±5% power supply

Pin #	Signal	Input/ Output	Description
93 (D3)	AD03	T/S	Address and Data Bus Lines 3 – Refer to Pin 3 for more information.
94 (D4)	AD06	T/S	Address and Data Bus Lines 6 – Refer to Pin 3 for more information.
95 (D5)	GND		Digital Ground
96 (D6)	GND		Digital Ground
97 (D7)	AD12	T/S	Address and Data Bus Line 12 – Refer to Pin 3 for more information.
98 (D8)	+3.3V		+3.3 volts ±5% power supply
99 (D9)	PAR	T/S	Parity bit – This signal is the even parity bit on AD[31:0] and C/BE[3:0]*
100 (D10)	SDONE		Snoop Done – Not used (10k Pull-up resistor to 3.3V)
101 (D11)	GND		Digital Ground
102 (D12)	DevSel*	S/T/S	Device Select – This signal is driven by the target device when its address is decoded.
103 (D13)	+3.3V		+3.3 volts ±5% power supply
104 (D14)	C/BE2*		Command/Byte Enable 2 – Refer to Pin 4 for more information.
105 (D15)	GND		Digital Ground
106 (D16)	AD19	T/S	Address and Data Bus Line 19 – Refer to Pin 3 for more information.
107 (D17)	+3.3V		+3.3 volts ±5% power supply
108 (D18)	IDSEL2		Initialization Device Select 2 – Refer to Pin 18 for more information.
109 (D19)	IDSEL3		Initialization Device Select 3 – Refer to Pin 18 for more information.
110 (D20)	GND		Digital Ground
111 (D21)	AD27	T/S	Address and Data Bus Line 27 – Refer to Pin 3 for more information.
112 (D22)	AD31	T/S	Address and Data Bus Line 31 – Refer to Pin 3 for more information.
113 (D23)	VI/O		+5 volts ±5% power supply
114 (D24)	GNT0*	T/S	Grant 0 – Refer to Pin 25 for more information.
115 (D25)	GND		Digital Ground
116 (D26)	CLK1	In	PCI clock 1 – Refer to Pin 27 for more information
117 (D27)	GND		Digital Ground
118 (D28)	RST*	In	PCI bus reset – This output signal resets the entire PCI Bus. This signal will be asserted during a system reset.
119 (D29)	INTC*	O/D	Interrupt C – This signal only request interrupts for multi-function devices.
120 (D30)	GND		Digital Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

The Input/Output signals in this table refer to the input/output signals listed in the *PCI Local Bus Manual*, Revision 2.2, Chapter 2, paragraph 2.1, Signal definitions. The following terms or acronyms are used in this table:

- In – Input is standard input only signal
- Out – Totem Pole output is a standard active driver
- T/S – Tri-State is a bi-directional input output pin
- S/T/S – Sustained Tri-State is an active low tri-state signal driven by one and only one agent at a time
- O/D – Open Drain allows multiple devices to share as a wire-OR.

PC/104 Bus Interface (P1A,B,C,D)

The PC/104 Bus uses a 104-pin 100 mil header interface. This interface header carries all of the appropriate ISA bus signals over the PC/104 bus, while operating at clock speeds up to 8MHz. The interface header is located on both the top and bottom of the board.

Table 3-5. PC/104 Bus Interface Pin/Signal Descriptions (P1A)

Pin #	Signal	Description (P1 Row A)
1 (A1)	IOCHCHK*	I/O Channel Check – This signal may be activated by ISA boards to request that a non-maskable interrupt (NMI) be generated to the system processor. It is driven active to indicate an uncorrectable error has been detected.
2 (A2)	SD7	System Data 7 – This signal (0 to 19) provides a system data bit.
3 (A3)	SD6	System Data 6 – Refer to SD7, pin A2, for more information.
4 (A4)	SD5	System Data 5 – Refer to SD7, pin A2, for more information.
5 (A5)	SD4	System Data 4 – Refer to SD7, pin A2, for more information.
6 (A6)	SD3	System Data 3 – Refer to SD7, pin A2, for more information.
7 (A7)	SD2	System Data 2 – Refer to SD7, pin A2, for more information.
8 (A8)	SD1	System Data 1 – Refer to SD7, pin A2, for more information.
9 (A9)	SD0	System Data 0 – Refer to SD7, pin A2, for more information.
10 (A10)	IOCHRDY	I/O Channel Ready – This signal allows slower ISA boards to lengthen I/O or memory cycles by inserting wait states. This signal's normal state is active high (ready). ISA boards drive the signal inactive low (not ready) to insert wait states. Devices using this signal to insert wait states should drive it low immediately after detecting a valid address decode and an active read, or write command. The signal is released high when the device is ready to complete the cycle.
11 (A11)	AEN	Address Enable – This signal is used to degate the system processor and other devices from the bus during DMA transfers. When this signal is active, the system DMA controller has control of the address, data, and read/write signals. This signal should be included as part of ISA board select decodes to prevent incorrect board selects during DMA cycles.
12 (A12)	SA19	System Address 19 – This signal (0 to 19) provides a system address bit.
13 (A13)	SA18	System Address 18 – Refer to SA19, pin A12, for more information.
14 (A14)	SA17	System Address 17 – Refer to SA19, pin A12, for more information.
15 (A15)	SA16	System Address 16 – Refer to SA19, pin A12, for more information.
16 (A16)	SA15	System Address 15 – Refer to SA19, pin A12, for more information.
17 (A17)	SA14	System Address 14 – Refer to SA19, pin A12, for more information.
18 (A18)	SA13	System Address 13 – Refer to SA19, pin A12, for more information.
19 (A19)	SA12	System Address 12– Refer to SA19, pin A12, for more information.
20 (A20)	SA11	System Address 11 – Refer to SA19, pin A12, for more information.
21 (A21)	SA10	System Address 10 – Refer to SA19, pin A12, for more information.
22 (A22)	SA9	System Address 9 – Refer to SA19, pin A12, for more information.
23 (A23)	SA8	System Address 8 – Refer to SA19, pin A12, for more information.
24 (A24)	SA7	System Address 7 – Refer to SA19, pin A12, for more information.

Pin #	Signal	Description (P1 Row A)
25 (A25)	SA6	System Address 6 – Refer to SA19, pin A12, for more information.
26 (A26)	SA5	System Address 5 – Refer to SA19, pin A12, for more information.
27 (A27)	SA4	System Address 4 – Refer to SA19, pin A12, for more information.
28 (A28)	SA3	System Address 3 – Refer to SA19, pin A12, for more information.
29 (A29)	SA2	System Address 2 – Refer to SA19, pin A12, for more information.
30 (A30)	SA1	System Address 1 – Refer to SA19, pin A12, for more information.
31 (A31)	SA0	System Address 0 – Refer to SA19, pin A12, for more information.
32 (A32)	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-6. PC/104 Bus Interface Pin/Signal Descriptions (P1B)

Pin #	Signal	Descriptions (P1 Row B)
33 (B1)	GND	Ground
34 (B2)	RESETDRV	Reset Drive – This signal is used to reset or initialize system logic on power up or subsequent system reset.
35 (B3)	+5V	+5V power +/- 10%
36 (B4)	IRQ9	Interrupt request 9 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
37 (B5)	NC	Not connected (-5 volts)
38 (B6)	DRQ2	DMA Request 2 – Used by I/O resources to request DMA service, or to request ownership of the bus as a bus master device. Must be held high until associated DACK2 line is active.
39 (B7)	NC	Not connected (-12 volts)
40 (B8)	ENDXFR*	Zero Wait State – This signal is driven low by a bus slave device to indicate it is capable of performing a bus cycle without inserting any additional wait states. To perform a 16-bit memory cycle without wait states, this signal is derived from an address decode.
41 (B9)	+12V	+12 Volts
42 (B10)	NC	Not connected (Key Pin)
43 (B11)	SMEMW*	System Memory Write – This signal is used by bus owner to request a memory device to store data currently on the data bus and only active for the lower 1MB. Used for legacy compatibility with 8-bit cards.
44 (B12)	SMEMR*	System Memory Read – This signal is used by bus owner to request a memory device to drive data onto the data bus and only active for lower 1MB. Used for legacy compatibility with 8-bit cards.
45 (B13)	IOW*	I/O Write – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to capture the write data on the data bus.
46 (B14)	IOR*	I/O Read – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to drive read data onto the data bus.
47 (B15)	DACK3*	DMA Acknowledge 3 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.

Pin #	Signal	Descriptions (P1 Row B)
48 (B16)	DRQ3	DMA Request 3 – Used by I/O resources to request DMA service. Must be held high until associated DACK3 line is active.
49 (B17)	DACK1*	DMA Acknowledge 1 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
50 (B18)	DRQ1	DMA Request 1 – Used by I/O resources to request DMA service. Must be held high until associated DACK1 line is active.
51 (B19)	REFRESH*	Memory Refresh – This signal is driven low to indicate a memory refresh cycle is in progress. Memory is refreshed every 15.6 usec.
52 (B20)	SYSCLK	System Clock – This is a free running clock typically in the 8MHZ to 10MHz range, although its exact frequency is not guaranteed.
53 (B21)	IRQ7	Interrupt Request 7 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
54 (B22)	IRQ6	Interrupt Request 6 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
55 (B23)	IRQ5	Interrupt Request 5 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
56 (B24)	IRQ4	Interrupt Request 4 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
57 (B25)	IRQ3	Interrupt Request 3 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
58 (B26)	DACK2*	DMA Acknowledge 2 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
59 (B27)	TC	Terminal Count – This signal is a pulse to indicate a terminal count has been reached on a DMA channel operation.
60 (B28)	BALE	Buffered Address Latch Enable – This signal is used to latch the LA23 to LA17 signals or decodes of these signals. Addresses are latched on the falling edge of BALE. It is forced high during DMA cycles. When used with AENx, it indicates a valid processor or DMA address.
61 (B29)	+5V	+5V power +/- 10%
62 (B30)	OSC	Oscillator – This clock signal operates at 14.3MHz. This signal is not synchronous with the system clock (SYSCLK).
63 (B31)	GND	Ground
64 (B32)	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-7. PC/104 Bus Interface Pin/Signal Descriptions (P1C)

Pin #	Signal	Descriptions (P1 Row C)
1 (C0)	GND	Ground
2 (C1)	SBHE*	System Byte High Enable – This signal is driven low to indicate a transfer of data on the high half of the data bus (D15 to D8).
3 (C2)	LA23	Lactchable Address 23 – This signal must be latched by the resource if the line is required for the entire data cycle.
4 (C3)	LA22	Lactchable Address 22 – Refer to LA23, pin C2, for more information.

Pin #	Signal	Descriptions (P1 Row C)
5 (C4)	LA21	Lactchable Address 21 – Refer to LA23, pin C2, for more information.
6 (C5)	LA20	Lactchable Address 20 – Refer to LA23, pin C2, for more information.
7 (C6)	LA19	Lactchable Address 19 – Refer to LA23, pin C2, for more information.
8 (C7)	LA18	Lactchable Address 18 – Refer to LA23, pin C2, for more information.
9 (C8)	LA17	Lactchable Address 17 – Refer to LA23, pin C2, for more information.
10 (C9)	MEMR*	Memory Read – This signal instructs a selected memory device to drive data onto the data bus. It is active on all memory read cycles.
11 (C10)	MEMW*	Memory Write – This signal instructs a selected memory device to store data currently on the data bus. It is active on all memory write cycles.
12 (C11)	SD8	System Data 8 – Refer to SD7, pin A2, for more information.
13 (C12)	SD9	System Data 9 – Refer to SD7, pin A2, for more information.
14 (C13)	SD10	System Data 10 – Refer to SD7, pin A2, for more information.
15 (C14)	SD11	System Data 11 – Refer to SD7, pin A2, for more information.
16 (C15)	SD12	System Data 12 – Refer to SD7, pin A2, for more information.
17 (C16)	SD13	System Data 13 – Refer to SD7, pin A2, for more information.
18 (C17)	SD14	System Data 14 – Refer to SD7, pin A2, for more information.
19 (C18)	SD15	System Data 15 – Refer to SD7, pin A2, for more information.
20 (C19)	NC	Key Pin

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-8. PC/104 Bus Interface Pin/Signal Descriptions (P1D)

Pin #	Signal	Descriptions (P1 Row D)
21 (D0)	GND	Ground
22 (D1)	MEMCS16*	Memory Chip Select 16 – This is signal is driven low by a memory slave device to indicates it is cable of performing a 16-bit memory data transfer. This signal is driven from a decode of the LA23 to LA17 address lines.
23 (D2)	IOCS16*	I/O Chip Select 16 – This signal is driven low by an I/O slave device to indicate it is capable of performing a 16-bit I/O data transfer. This signal is driven from a decode of the SA15 to SA0 address lines.
24 (D3)	IRQ10	Interrupt Request 10 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
25 (D4)	IRQ11	Interrupt Request 11 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
26 (D5)	IRQ12	Interrupt Request 12 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
27 (D6)	IRQ15	Interrupt Request 15 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
28 (D7)	IRQ14	Interrupt Request 14 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
29 (D8)	DACK0*	DMA Acknowledge 0 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
30 (D9)	DRQ0	DMA Request 0 – Used by I/O resources to request DMA service. Must be held high until associated DACK0 line is active.

Pin #	Signal	Descriptions (P1 Row D)
31 (D10)	DACK5*	DMA Acknowledge 5 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
32 (D11)	DRQ5	DMA Request 5 – Used by I/O resources to request DMA service. Must be held high until associated DACK5 line is active.
33 (D12)	DACK6*	DMA Acknowledge 6 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
34 (D13)	DRQ6	DMA Request 6 – Used by I/O resources to request DMA service. Must be held high until associated DACK6 line is active.
35 (D14)	DACK7*	DMA Acknowledge 7 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
36 (D15)	DRQ7	DMA Request 7 – Used by I/O resources to request DMA service. Must be held high until associated DACK7 line is active.
37 (D16)	+5V	+5V Power +/- 10%
38 (D17)	MASTER*	Bus Master Assert – This signal is used by an ISA board along with a DRQ line to gain ownership of the ISA bus. Upon receiving a -DACK a device can pull -MASTER low which will allow it to control the system address, data, and control lines. After -MASTER is low, the device should wait one CLK period before driving the address and data lines, and two clock periods before issuing a read or write command.
39 (D18)	GND	Ground
40 (D19)	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

IDE Interface (J2)

The IDE device signals are provided through the standard 40-pin connector (J2). The Ultra DMA-33/66/100 Master Mode EIDE interface logic supports the following features:

- Increased reliability using Ultra DMA-33/66/100 transfer protocols
- Full scatter-gather capability
- Supports ATAPI and DVD compliant devices
- Supports PIO IDE transfers up to 14Mbps
- Single Bus master EIDE with transfers up to 100Mbps.

Table 3-9 gives the pins and signals for the standard IDE 40-pin connector.

Table 3-9. IDE Interface Pin/Signal Descriptions (J2)

Pin #	Signal	Description
1	Reset*	Reset – Low active hardware reset (RSTDRV inverted)
2	GND	Digital Ground
3	D7	Disk Data – These signals (0 to 15) provide the disk data signals
4	D8	Disk Data 8 – Refer to D7, pin 3, for more information.
5	D6	Disk Data 6 – Refer to D7, pin 3, for more information.
6	D9	Disk Data 9 – Refer to D7, pin 3, for more information.
7	D5	Disk Data 5 – Refer to D7, pin 3, for more information.
8	D10	Disk Data 10 – Refer to D7, pin 3, for more information.
9	D4	Disk Data 4 – Refer to D7, pin 3, for more information.
10	D11	Disk Data 11 – Refer to D7, pin 3, for more information.
11	D3	Disk Data 3 – Refer to D7, pin 3, for more information.
12	D12	Disk Data 12 – Refer to D7, pin 3, for more information.
13	D2	Disk Data 2 – Refer to D7, pin 3, for more information.
14	D13	Disk Data 13 – Refer to D7, pin 3, for more information.
15	D1	Disk Data 1 – Refer to D7, pin 3, for more information.
16	D14	Disk Data 14 – Refer to D7, pin 3, for more information.
17	D0	Disk Data 0 – Refer to D7, pin 3, for more information.
18	D15	Disk Data 15 – Refer to D7, pin 3, for more information.
19	GND	Digital Ground
20	GND	Digital Ground
21	DMARQ	DMA Request – Used for DMA transfers between host and drive (direction of transfer controlled by DIOR* and DIOW*). Also used in an asynchronous mode with DMACK*. Drive asserts IDRQ0 when ready to transfer or receive data.
22	GND	Digital Ground
23	DIOW*	Drive I/O Write – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
24	GND	Digital Ground

Pin #	Signal	Description
25	DIOR*	Drive I/O Read – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
26	GND	Digital Ground
27	IORDY	I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
28	CSEL	Cable Select – Used to configure IDE drives as device 0 or device 1 using a special cable.
29	DMACL*	DMA Channel Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to DMARQ asserted.
30	GND	Digital Ground
31	IRQ14	Drive Interrupt Request (IRQ 14) – Asserted by drive when it has pending interrupt (PIO transfer of data to or from the drive to the host).
32	NC	Not Connected
33	DA1	Drive Address Bus 1 – Used (0 to 2) to indicate which byte in the ATA command block or control block (register) is being accessed.
34	PDIAG*	Passed Diagnostics – Output from drive 1 and monitored by drive 0. Provides an indication of the results of a diagnostics command or reset.
35	DA0	Drive Address Bus 0 – Used (0 to 2) to indicate which byte in the ATA command block or control block (register) is being accessed.
36	DA2	Drive Address Bus 2 – Used (0 to 2) to indicate which byte in the ATA command block or control block (register) is being accessed.
37	CS0*	Chip Select 0 – Used to select the host-accessible Command Block Register.
38	CS1*	Chip Select 1 – Used to select the host-accessible Command Block Register.
39	DASP*	Drive Active/Drive Present – This signal indicates drive activity or that drive 1 is present. This is a time-multiplexed signal, which is first asserted by drive 1 (if present) and then by drive 0 (to drive an activity LED).
40	GND	Digital Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

NOTE	For maximum reliability keep IDE drive cables less than 12 inches long.

CompactFlash Socket (J3)

The CoreModule 600 provides a Type I or Type II PC card socket, which allows for the insertion of a CompactFlash card. The CompactFlash card acts as a IDE Drive connected to primary IDE channel.

Table 3-10. Compact Flash Interface Pin/Signal Descriptions (J3)

Pin #	Signal	Description
1	GND	Digital Ground
2	D3	Disk Data 3 – These signals (D0-D15) carry the Data, Commands, and Status between the host and the controller. D0 is the LSB of the even Byte of the Word. D8 is the LSB of the Odd Byte of the Word. All Task File operations occur in byte mode on the low order bus D0-D7, while all data transfers are 16 bit using D0-D15 provide the disk data signals.
3	D4	Disk Data 4 – Refer to D3 on pin-2 for more information.
4	D5	Disk Data 5 – Refer to D3 on pin-2 for more information.
5	D6	Disk Data 6 – Refer to D3 on pin-2 for more information.
6	D7	Disk Data 7 – Refer to D3 on pin-2 for more information.
7	CS0*	Card Enable 0 – This signal, along with CE1*, is used to select the card and indicate to the card when a byte or word operation is being performed. This signal accesses the even byte or odd byte of the word depending on A0 and CE1*.
8, 9, 10	GND	Digital Ground
11, 12	GND	Digital Ground
13	Vcc1	This voltage (+5V or +3.3V) is determined by jumper JP5 setting. If jumper set to pins 1-2 = +5V. If jumper set to pins 2-3 = +3.3V.
14, 15,	GND	Digital Ground
16, 17	GND	Digital Ground
18	A2	Address Select 2 – One of three signals (0 – 2) used to select one of eight registers in the Task File. The host grounds all remaining address lines.
19	A1	Address Select 1 – Refer to A2 on pin-18 for more information.
20	A0	Address Select 0 – Refer to A2 on pin-18 for more information.
21	D0	Disk Data 0 – Refer to D3 on pin-2 for more information.
22	D1	Disk Data 1 – Refer to D3 on pin-2 for more information.
23	D2	Disk Data 2 – Refer to D3 on pin-2 for more information.
24	NC	Not connected (IOCS16*)
25	GND	Digital Ground
26	NC	Not connected (CD1)
27	D11	Disk Data 11 – Refer to D3 on pin-2 for more information.
28	D12	Disk Data 12 – Refer to D3 on pin-2 for more information.
29	D13	Disk Data 13 – Refer to D3 on pin-2 for more information.
30	D14	Disk Data 14 – Refer to D3 on pin-2 for more information.

Pin #	Signal	Description
31	D15	Disk Data 15 – Refer to D3 on pin-2 for more information.
32	CE1*	Card Enable 1 – This signal, along with CE0*, is used to select the CompactFlash card and indicate to the card when a byte or word operation is being performed. This signal always accesses the odd byte of the word.
33	GND	Grounded (VS1*)
34	IOR*	I/O Read Strobe – This signal is generated by the host and gates the I/O data onto the bus from the CompactFlash card when the card is configured to use the I/O interface.
35	IOW*	I/O Write Strobe – This signal is generated by the host and clocks the I/O data on the Card Data bus into the CompactFlash card controller registers when the card is configured to use the I/O interface. The clock occurs on the negative to positive edge of the signal (trailing edge).
36	NU	Not Used – This signal (WE) is connected to Vcc through 10k ohm resistor.
37	IRQ14	Drive Interrupt Request – IRQ 14 is asserted by drive (CF) when it has a pending interrupt (PIO transfer of data to or from the drive to the host).
38	Vcc2	This voltage (+5V or +3.3V) is determined by jumper JP5 setting. If jumper set to pins 1-2 = +5V. If jumper set to pins 2-3 = +3.3V (**Default**).
39	CSEL	Card Select – This signal is determined by jumper JP4 and is used to configure this device as a Master or a Slave. When this pin is grounded (jumper inserted), this device is configured as Master. When this pin is open (jumper removed), this device is configured as Slave (**Default**).
40	NC	Not Connected (VS2*)
41	IDERst*	IDE Reset – This input signal is the active low hardware reset from the host. If this pin goes high, it is used as the reset signal. This pin is driven high at power-up, causing a reset, and if left high will cause another reset.
42	IORDY	I/O Channel Ready – When negated, extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
43	NC	Not Connected (InpAck)
44	NU	Not Used – This signal (REG*) is connected to Vcc through 10k ohm resistor.
45	DASP*	Drive Active/Slave Present – This input/output signal is used in the Master/Slave handshake protocol.
46	PDiag*	Passed Diagnostics – This signal is used in the Master/Slave handshake protocol. It indicates the results of a diagnostics command or reset.
47	D8	Disk Data 8 – Refer to D3 on pin-2 for more information.
48	D9	Disk Data 9 – Refer to D3 on pin-2 for more information.
49	D10	Disk Data 10 – Refer to D3 on pin-2 for more information.
50	NC	Not Connected (CD2)

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.
NC = Not connected, NU = Not used.

Utility Interface (J5)

The utility interface consists of the 80-pin connector (J5) on the board and is used as the interface for various utility signals. Tables 3-11 through 3-16 give a simplified description of each port or device interface in the utility connector, while Table 3-17 gives all of the interface signals in the utility connector (J5).

- Floppy Drive interface (Table 3-11)
- Parallel interface (Table 3-12)
- Serial interface (Table 3-13)
- USB interface (Table 3-14)
- Keyboard and Mouse PS/2 Controller (Table 3-15)
- Battery (Table 3-15)
- Reset Switch (Table 3-15)
- Speaker (Table 3-15)

Floppy Drive Interface

The Southbridge chip (VT82C686B) provides the floppy controller and supports one floppy drive. The floppy drive signals are provided through the 80-pin Utility connector (J5).

NOTE	Due to the shared nature of the signal pins for the floppy disk drive and parallel port, you can only connect one of these devices at the same time.

Table 3-11. Simplified Floppy Drive Interface Pin/Signal Descriptions (J5)

J5 Pin #	Signal	Floppy Cable	Description
4	DRVEN0*	2	Drive (Floppy) Density Select 0
54	NC	4	Not connected
NC	KEY	6	Key – Not connected
6	INDEX*	8	Index – Sense to detect that the head is positioned over the beginning of a track
NC	MTR0*	10	Motor Control 0 – Select motor on drive 0.
38	DS1*	12	Drive Select 1 – Select drive 1.
NC	DS0*	14	Drive Select 0 – Select drive 0.
42	MTR1*	16	Motor Control 1 – Select motor on drive 1.
12	DIR*	18	Direction – Direction of head movement (0 = inward motion, 1 = outward motion).
16	STEP*	20	Step – Low pulse for each track-to-track movement of the head.
46	WDATA*	22	Write Data – Encoded data to the drive for write operations.
50	WGATE*	24	Write Gate – Signal to the drive to enable current flow in the write head.
10	TRK0*	26	Track 0 – Sense detects the head is positioned over track 0.
14	WRTPRT*	28	Write Protect – Senses the diskette is write protected.

J5 Pin #	Signal	Floppy Cable	Description
18	RDATA*	30	Read Data – Raw serial bit stream from the drive for read operations.
8	HDSEL*	32	Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
22	DSKCHG*	34	Disk Change – Senses the drive door is open or the diskette has been changed since the last drive selection.
20, 24, 28, 32, 36, 40, 44, 48,	GND	1-33 (all odd)	Digital Ground

Notes: The shaded area denotes power or ground. The signals marked with * indicate active low.

Parallel Interface

Parallel port supports standard parallel, Bi-directional, ECP and EPP protocols. The Southbridge chip (VT82C686B) provides the parallel port interface signals to support a Standard Printer Port (SPP), Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP) protocols. The parallel port signals are provided through the 80-pin Utility connector (J5) and multiplexed with the floppy drive signals.

Table 3-12. Simplified Parallel Interface (SPP) Pin/Signal Descriptions (J5)

J5 Pin #	Signal	DB25 Pin #	Description
2	Strobe*	1	Strobe* – This output signal is used to strobe data into the printer. I/O pin in ECP/EPP mode.
6	PD0	2	Parallel Port Data 0 – This pin (0 to 7) provides a parallel port data signal and is the LSB of printer data.
10	PD1	3	Parallel Port Data 1 – Refer to pin 6 (J5) for more information.
14	PD2	4	Parallel Port Data 2 – Refer to pin 6 (J5) for more information.
18	PD3	5	Parallel Port Data 3 – Refer to pin 6 (J5) for more information.
22	PD4	6	Parallel Port Data 4 – Refer to pin 6 (J5) for more information.
26	PD5	7	Parallel Port Data 5 – Refer to pin 6 (J5) for more information.
30	PD6	8	Parallel Port Data 6 – Refer to pin 6 (J5) for more information.
34	PD7	9	Parallel Port Data 7 – This pin (0 to 7) provides a parallel port data signal and is the MSB of printer data.
38	ACK*	10	Acknowledge * – This is a status input signal from the printer. A Low State indicates it has received the data and is ready to accept new data.
42	BUSY	11	Busy – This is a status input signal from the printer. A high state indicates the printer is not ready to accept data.
46	PE	12	Paper End – This is a status input signal from the printer. A high state indicates it is out of paper.
50	SLCT	13	Select – This is a status output signal from the printer. A high state indicates it is selected and powered on.
4	AUTOFDX*	14	Auto Feed * – This is a output signal from the printer to automatically feed one line after each line is printed.
8	ERR*	15	Error – This is a status output signal from the printer. A low state indicates an error condition on the printer.

J5 Pin #	Signal	DB25 Pin #	Description
12	INIT*	16	Initialize * – This signal initializes the printer. Output in standard mode, I/O in ECP/EPP mode.
16	SLCTIN	17	Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode.
20, 24, 28, 32, 36, 40, 44, 48	GND	18-25	Digital Ground

Notes: The shaded area denotes power or ground. The signals marked with * indicate active low.

Serial Interface

The Southbridge chip (VT82C686B) contains the circuitry for the two serial ports. The two serial port signals are provided through the 80-pin Utility connector (J5). The two serial ports support the following features:

- Both ports are 16550 compatible
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate and Interrupt generator
- Loop-back mode
- Two 16-bit FIFOs
- Two DMA handshake lines
- Serial 1 (COM 1) supports RS232, RS485, and full modem support
- Serial 2 (COM 2) supports RS232 and TTL output drive signal

Table 3-13. Simplified Serial Interface (Ports 1 & 2) Pin/Signal Descriptions (J5)

J5 Pin #	Signal	DB25 Pin #	DB9 Pin #	Description
1	DCD1*	8	1	Data Carrier Detect 1 – Indicates external modem is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR1 as part of the DTR1/DSR1 handshake.
3	DSR1*	6	6	Data Set Ready 1 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate.
5	RXD1 RX1-	3	2	Serial Port Receive Data 1 Input – This line is typically held at a logic 1 (mark) when no data is being transmitted, and is held "Off" for a brief interval after an "On" to "Off" transition on the RTS1 line to allow the transmission to complete. Receive Data 1 - – If in RS485 mode, this pin is RX1-.
7	RTS1* TX1+	4	7	Request To Send 1 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control. Transmit Data 1 + – If in RS485 mode, this pin is TX1+.

J5 Pin #	Signal	DB25 Pin #	DB9 Pin #	Description
9	TXD1 TX1-	2	3	Serial Port Transmit Data 1 Output – This line is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS1, CTS1, DSR1, and DTR1 before data can be transmitted on this line. Transmit Data 1 - – If in RS485 mode, this pin is TX1-.
11	CTS1* RX1+	5	8	Clear To Send 1 – Indicates external serial communication device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control. Receive Data 1 - – If in RS485 mode, this pin is RX1+.
13	DTR1*	20	4	Data Terminal Ready 1 – Indicates port is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
15	RI1*	22	9	Ring Indicator 1 – Indicates external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
17	GND	7	5	Digital Ground
19	NC	NC	NC	Not Connected
21	DCD2*	8	1	Data Carrier Detect 2 – Indicates external modem is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR2 as part of the DTR2/DSR2 handshake.
23	DSR2*	6	6	Data Set Ready 2 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate.
25	RXD2	3	2	Serial Port Receive Data 2 Input – This line is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS2 line to all the transmission to complete.
27	RTS2*	4	7	Request To Send 2 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
29	TXD2	2	3	Serial Port Transmit Data 2 Output – This line is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS2, CTS2, DSR2, and DTR2 before transmitting data on this line.
31	CTS2*	5	8	Clear To Send 2 – Indicates external serial communication device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
33	DTR2*	20	4	Data Terminal Ready 2 – Indicates port is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
35	RI2*	22	9	Ring Indicator 2 – Indicates external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
37	GND	7	5	Digital Ground
39	TXD2_ TTL	NC	NC	Serial Transmit Data 2 – Serial port 2 TTL transmit data output signal (jumpered to pin 3 DB9 connector on I/O Board).

Notes: The shaded area denotes power or ground. The signals marked with * indicate active low.

USB Interface

The CoreModule 600 supports one root USB (Universal Serial Bus) hub and two functional USB ports. The USB ports includes over-current detection status (software). The two USB port signals are provided through the 80-pin Utility connector (J5).

Features implemented in the USB port include the following:

- One root hub and two USB ports
- USB v.1.1 and Universal OHCI v.1.1 compatible
- Integrated physical layer transceivers
- Over current detection status on both USB ports (Southbridge function)
- No over current fuses located on the CoreModule 600

Table 3-14. Simplified USB Interface Pin/Signal Descriptions (J5)

J5 Pin #	Signal	Description
41	USBPS0	USB Port 0 Power Protection – Port is disabled if this input is low. Direct inputs are provided for over current protection.
43	USBPWR0	USB Port 0 power
45	USBPN	Universal Serial Bus Port 0 Data –
47	USBPP	Universal Serial Bus Port 0 Data +
49	GND	USB Port ground
51	USBPS1	USB Port 1 Power Protection – Port is disabled if this input is low. Direct inputs are provided for over current protection.
53	USBPWR1	USB Port 0 power
55	USBPN	Universal Serial Bus Port 1 Data –
57	USBPP	Universal Serial Bus Port 1 Data +
59	GND	USB Port ground

Notes: The shaded area denotes power or ground.

Keyboard Interface

The signal lines for a PS/2 keyboard are provided through the Utility interface (J5), which is also fully PC/AT compatible.

Mouse Interface

The signal lines for a PS/2 mouse are provided through the Utility interface (J5).

Battery Interface

An external battery input connection is provided through the Utility interface (J5) to provide battery backup for the CMOS RAM and the RTC (Real Time Clock).

Reset Switch Interface

The signal lines for a reset switch (hard or soft) are provided through the Utility interface (J5).

Speaker Interface

The speaker enable signal is provided through the Utility interface (J5), but an external drive circuit is required for the speaker signal.

Table 3-15. Simplified Keyboard, Mouse, and Miscellaneous Interface Pin/Signal Descriptions (J5)

J5 Pin #	Signal	Description
61	MOU Data	Mouse Data
63	MOU Clk	Mouse Clock
65	GND	Ground
67	MOU Pwr	Mouse Power (+5V)
62	SPKR+	Speaker + Output
64	GND	Ground
66	RESET SW	Reset Switch
68	KBD SW	Keyboard switch – Not used
70	KBD Data	Keyboard Data
72	KBD Clk	Keyboard Clock
74	GND	Digital Ground
76	KBD PWR	Keyboard power (+5V)
78	BATV+	External Backup Battery +
80	BATV-	External Backup Battery Return -

Notes: The shaded area denotes power or ground.

Table 3-16. Complete Utility Interface Pin/Signal Descriptions (J5)

Pin #	Signal	Description
1	S1 – DCD1*	Serial 1 Data Carrier Detect 1 – Indicator to serial port that external modem is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR1 as part of the DTR/DSR handshake.
2	PP – Strobe*	Parallel Port Strobe – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode.
3	S1 – DSR1*	Serial 1 Data Set Ready 1 – Indicator to serial port that external serial communications device is powered on, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate.
4	PP – AutoFD* FP – DrvDen0	Parallel Auto Feed – This is a request signal into the printer to automatically feed one line after each line is printed. Floppy Drive Density Select 0 –
5	S1 – RXD1 S1 – RX1-	Serial 1 Receive Data 1– Serial port receive data input. This line is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS1 line to allow the transmission to complete. Receive Data 1 - – If in RS485 mode, this pin is RX1-.
6	PP – PD0 FP – INDEX*	Parallel Data 0 – These signals (0 to 7) provide the parallel port data to the printer. Floppy Index – Sense to detect the head is positioned over the beginning of a track

Pin #	Signal	Description
7	S1 – RTS1*	Serial 1 Request To Send 1 – Serial port output indicates port is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.
	S1 – TX1+	Transmit Data 1 + – If in RS485 mode, this pin is TX1+.
8	PP – ERR*	Parallel Error – This is a status output signal from the printer. A Low State indicates an error condition on the printer.
	FP – HDSel*	Floppy Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
9	S1 – TXD1	Serial 1 Transmit Data 1 Output – This line is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS1, CTS1, DSR1, and DTR1 before data can be transmitted on this line.
	S1 – TX1-	Transmit Data 1 - – If in RS485 mode, this pin is TX1-.
10	PP – PD1	Parallel Data 1 – Refer to PD0, pin 6, for more information.
	FP – Trk0	Floppy Track 0 – Sense detects the head is positioned over track 0.
11	S1 – CTS1*	Serial 1 Clear To Send 1 – Indicator to serial port that external serial communications device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
	S1 – RX1+	Receive Data 1 - – If in RS485 mode, this pin is RX1+.
12	PP – Init*	Parallel Initialize – This signal is used to initialize printer. Output in standard mode, I/O in ECP/EPP mode.
	FP – Dir*	Floppy Direction – Direction of floppy head movement (0 = inward motion, 1 = outward motion).
13	S1 – DTR1*	Serial 1 Data Terminal Ready 1 – Serial port output indicates port is powered on, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
14	PP – PD2	Parallel Port Data 2 – Refer to PD0, pin 6, for more information.
	FP – WrtPrt*	Floppy Port Write Protect – Senses the diskette is write protected.
15	S1 – RI1*	Serial 1 Ring Indicator 1 – Indicator to serial port that external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
16	PP – SlctIn*	Parallel Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode.
	FP – Step*	Step – Low pulse for each track-to-track movement of the floppy head.
17	S1 – GND	Serial 1 Digital Ground
18	PP – PD3	Parallel Data 3 – Refer to PD0, pin 6, for more information.
	FP – RData*	Floppy Read Data – Raw serial bit stream from the drive for read operations.
19	NC	Not Connected
20	PP – GND	Parallel Port Digital Ground
	FP – GND	Floppy Port Digital Ground
21	S2 – DCD2*	Serial 2 Data Carrier Detect 2 – Indicator to serial port that external modem is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR2 as part of the DTR/DSR handshake.

Pin #	Signal	Description
22	PP – PD4 FP – DskChg*	Parallel Data 4 – Refer to PD0, pin 6, for more information. Floppy Disk Change – Senses the drive door is open or the diskette has been changed since the last drive selection.
23	S2 – DSR2*	Serial 2 Data Set Ready 2 – Indicator to serial port that external serial communications device is powered on, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate.
24	PP – GND FP – GND	Parallel Digital Ground Floppy Digital Ground
25	S2 – RXD2	Serial 2 Receive Data 2– Serial port 2 receive data in
26	PP – PD5	Parallel Data 5 – Refer to PD0, pin 6, for more information.
27	S2 – RTS2*	Serial 2 Request To Send 2 – Serial port output indicates port is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
28	PP – GND FP – GND	Parallel Port Digital Ground Floppy Port Digital Ground
29	S2 – TXD2	Serial 2 Transmit Data 2 – Serial port 2 transmit data out
30	PP – PD6	Parallel Port Data 6 – Refer to PD0, pin 6, for more information.
31	S2 – CTS2*	Serial 2 Clear To Send 2 – Indicator to serial port that external serial communications device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
32	PP – GND FP – GND	Parallel Port Digital Ground Floppy Port Digital Ground
33	S2 – DTR2*	Serial 2 Data Terminal Ready 2 – Serial port output indicates port is powered on, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
34	PP – PD7	Parallel Port Data 7 – Refer to PD0, pin 6, for more information.
35	S2 – RI2*	Serial 2 Ring Indicator 2 – Indicates external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
36	PP – GND FP – GND	Parallel Digital Ground Floppy Digital Ground
37	S2 – GND	Serial 2 Digital Ground
38	PP – Ack* FP – DS1*	Parallel Acknowledge – This is a status output signal from the printer. A low state indicates it has received the data and is ready to accept new data. Floppy Drive Select 1 – Select drive 1.
39	S2 – TXD2_TTL	Serial 2 Transmit Data 2 – Serial port 2 transmit data out and TTL signals
40	PP – GND FP – GND	Parallel Digital Ground Floppy Digital Ground
41	USB – PS0*	USB 0 Power Protection – Port is disabled if this input is low. Direct inputs are provided for over current protection.
42	PP – Busy FP – Mtr1*	Parallel Printer Busy – This is a status output signal from the printer. A high state indicates the printer is not ready to accept data. Floppy Port Motor Control 1 – Select motor on drive 1.
43	USB – PWR0	Universal Serial Bus Port 0 power (+5V)

Pin #	Signal	Description
44	PP – GND FP – GND	Parallel Port Digital Ground Floppy Port Digital Ground
45	USB – P0-	Universal Serial Bus Port 0 Data –
46	PP – PE/ FP – WData*	Parallel Paper End – This is a status output signal from the printer. A high state indicates it is out of paper. Floppy Write Data – Encoded data to the drive for write operations.
47	USB – P0+	Universal Serial Bus Port 0 Data +
48	PP – GND FP – GND	Parallel Digital Ground Floppy Digital Ground
49	USB – GND	USB Ground
50	PP – Slct FP – WGate*	Parallel Select – This is a status output signal from the printer. A high state indicates it is selected and powered on. Floppy Write Gate – Signal to drive enabling current flow in the write head.
51	USB – PS1*	USB 1 Power Protection – Port is disabled if this input is low. Direct inputs are provided for over current protection.
52	IR – FIRMode	IR Function Mode Select – Terminated with 10k ohm resistor to ground.
53	USB – PWR	Universal Serial Bus power (+5V)
54	NC	Not Connected
55	USB – P1-	Universal Serial Bus Port 1 Data –
56	GND	Ground
57	USB – P1+	Universal Serial Bus Port 1 Data +
58	NU (IR-TX)	Not Used (IR Transmit Data)
59	USB – GND	USB Ground
60	NU (IR-RX)	Not Used (IR Receive Data)
61	MOU – DATA	Mouse Data
62	SPKR+	Speaker + Input drive signal
63	MOU – CLK	Mouse Clock
64	GND	Ground
65	GND	Ground
66	ResetSW	Reset Switch
67	MOU – PWR	Mouse Power (+5V +/-5%)
68	KBD – SW	Keyboard Switch – Not used
69	HD – ACTIVE	IDE Hard Drive Active – Signal for front panel HD activity LED
70	KBD – KBData	Keyboard Data line
71	NC	Not connected
72	KBD – KBCLK	Keyboard Clock line
73	NC	Not Connected
74	GND	Ground
75	NC	Not Connected
76	KBD – PWR	Keyboard Power (+5V +/-5%)
77	NC	Not Connected (-12 Volts)

Pin #	Signal	Description
78	BATV+	External Backup Battery +
79	NC	Not Connected (-5 Volts)
80	BATV-	External Backup Battery Return – (Grounded)

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

The following symbols identify the related signal interface.

- HD = EIDE Hard Disk
- IR = Infrared (not used)
- KBD = Keyboard
- MOU = PS/2 Mouse Port
- PP = Parallel Port
- S1 = Serial Port 1
- S2 = Serial Port 2
- USB = Universal Serial Bus

Ethernet Interface (J9)

The Ethernet solution is provided by the Intel 82551ER PCI controller chip and consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution. The 82551ER is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the 82551ER to perform high-speed data transfers over the internal PCI bus. The 82551ER bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU.

- Full duplex or half-duplex support
- Full duplex support at 10Mbps or 100Mbps
- In full duplex mode, the 82551ER adheres to the IEEE 802.3x Flow Control specification.
- In half-duplex mode, performance is enhanced by a proprietary collision reduction mechanism.
- IEEE 802.3 10BaseT/100BaseT compatible physical layer to wire transformer
- 3-function LED support (speed, link and activity)
- 10BaseT auto-polarity correction
- Data transmission with minimum interframe spacing (IFS)
- IEEE 802.3u Auto-Negotiation support
- 3kB transmit and 3kB receive FIFOs (helps prevent data underflow and overflow)
- IEEE 802.3x 100BASE-TX flow control support

Table 3-17 describes the pin-outs of the Ethernet connector J9.

Table 3-17. Ethernet Interface Pin/Signal Descriptions (J9)

Pin #	GND	Digital Ground
1	TX+	Digital Ethernet Transmit Pair – These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair Cable (UTP). These signals will interface directly to an isolation transformer (magnetics).
2	TX-	
3	PWR	+3.3 volt power
4	PWR	+3.3 volt power
5	RX+	Digital Ethernet Receive Pair – These pins receive the serial bit stream on the Unshielded Twisted Pair Cable (UTP) from the isolation transformer (magnetics).
6	RX-	
7	GND	Ground
8	LINK	Link LED signal
9	ACT	Activity LED signal
10	SPEED	Speed LED signal

Note: The shaded area denotes power or ground.

NOTE	The Ethernet connection requires an external isolation (wire) transformer (magnetics) on the baseboard, interface board, or mounting chassis. Ampro recommends placing the external isolation transformer as close to J9 as possible. For more information refer to the Intel 82551ER chip specifications mentioned earlier in this manual.

Video (CRT/LCD) Interface (J8)

The VT8606 chip provides the graphics control and video signals to the traditional glass CRT monitors and LCD/TFT flat panel displays. The chip features are listed below:

CRT features:

- Supports a max resolution of 1600 x 1200 x 8 with video frame buffer set at 8MB
- Supports a maximum allowable video frame buffer size of 32MB shared memory
- AGP 4X graphics (always enabled)
- Compliant with Rev 2.0 of AGP Interface

Flat Panel features:

- Supports (3.3V, 5V, or 12V) output to both DSTN and TFT flat panels through a 24-bit interface
- Supports TFT panel sizes from VGA (320x480) up to SXGA+ and UXGA+ (1400x1050).
- Supports LCD VGA and SVGA panels with 9-, 12-, 18-bit interface (1 Pixel/Clock)
- Supports UXGA and SXGA active matrix panels with 1x24-bit interface (2 Pixels/Clock)

The video interface (LCD/CRT) uses a 44-pin header shown in Table 3-18.

Table 3-18. Video Interface Pin/Signal Descriptions (J8)

Pin #	Signal	Description
1	SHFCLK	Shift Clock. – This signal provides the clock for transferring digital pixel data
2	M/DE	Data Enable – This signal is indicates valid data on any of the FP [23:0] lines.
3	LP	Line Pulse – This signal is the digital monitor equivalent of HSYNC
4	FLM	First Line Marker – This signal is digital monitor equivalent of VSYNC
5	GND	Digital Ground
6	GND	Digital Ground
7	FP0	Panel Data 0 – These signals (0 to 23) provide Digital pixel data output signals
8	FP1	Panel Data 1 – This signal provides a Digital pixel data output signal
9	FP2	Panel Data 2 – This signal provides a Digital pixel data output signal
10	FP3	Panel Data 3 – This signal provides a Digital pixel data output signal
11	FP4	Panel Data 4 – This signal provides a Digital pixel data output signal
12	FP5	Panel Data 5 – This signal provides a Digital pixel data output signal
13	FP6	Panel Data 6 – This signal provides a Digital pixel data output signal
14	FP7	Panel Data 7 – This signal provides a Digital pixel data output signal
15	FP8	Panel Data 8 – This signal provides a Digital pixel data output signal
16	FP9	Panel Data 9 – This signal provides a Digital pixel data output signal
17	FP10	Panel Data 10 – This signal provides a Digital pixel data output signal
18	FP11	Panel Data 11 – This signal provides a Digital pixel data output signal
19	FP12	Panel Data 12 – This signal provides a Digital pixel data output signal
20	FP13	Panel Data 13 – This signal provides a Digital pixel data output signal
21	FP14	Panel Data 14 – This signal provides a Digital pixel data output signal
22	FP15	Panel Data 15 – This signal provides a Digital pixel data output signal

Pin #	Signal	Description
23	FP16	Panel Data 16 – This signal provides a Digital pixel data output signal
24	FP17	Panel Data 17 – This signal provides a Digital pixel data output signal
25	FP18	Panel Data 18 – This signal provides a Digital pixel data output signal
26	FP19	Panel Data 19 – This signal provides a Digital pixel data output signal
27	FP20	Panel Data 20 – This signal provides a Digital pixel data output signal
28	FP21	Panel Data 21 – This signal provides a Digital pixel data output signal
29	FP22	Panel Data 22 – This signal provides a Digital pixel data output signal
30	FP23	Panel Data 23 – This signal provides a Digital pixel data output signal
31	ENAVDD	Enable Panel VDD Power – This signal is the power to Flat panel displays.
32	ENAVEE	Enable Panel VEE Power – This signal is the power to Flat panel displays.
33	PnLVdd	This voltage is determined by JP3. (+3.3 volts ±5% = pins 1-2 **Default,** +5V ±5% = pins 2-3)
34	+12V Out	+12 volts ±5% (From Power Connector by User)
35	GND	Digital Ground
36	GND	Digital Ground
37	HSYNC	Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT. Also used (with VSYNC) to signal power management state information to the CRT per the VESA™ DPMS™ standard.
38	VSYNC	Vertical Sync – This signal is used for the digital vertical sync output to the CRT. Also used (with HSYNC) to signal power management state information to the CRT per the VESA™ DPMS™ standard.
39	GNDR	Analog Ground for Red
40	RED	Red – This signal is the Red analog output to the CRT.
41	GNDG	Analog Ground for Green
42	GREEN	Green – This signal is the Green analog output to the CRT.
43	GNDB	Analog Ground for Blue
44	BLUE	Blue – This signal is the Blue analog output to the CRT.

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Miscellaneous

Real Time Clock (RTC)

The CoreModule 600 contains a Real Time Clock (RTC). The CMOS RAM is backed up with a Lithium Battery. If the battery is not present, the board BIOS has a battery-less boot option to complete the boot process.

Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event the BIOS settings you've selected prevents you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in the EEPROM from being loaded, allowing you to proceed, using the default settings. Connect the DTR pin to the RI pin on Serial Port 1 (COM 1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and go into BIOS Setup.

To restore your BIOS setting changes without the errors, you must first select *Load Factory Default Settings*, which will automatically load and save the defaults and reboot the system. Then you can modify the default settings to your desired values. Ensure you save the changes before rebooting the system.

NOTE	The CoreModule 600 uses pin 4 = DTR pin and pin 9 = RI pin on the Serial Port 1 connector (DB9, female end), as shown in Figure 3-1.

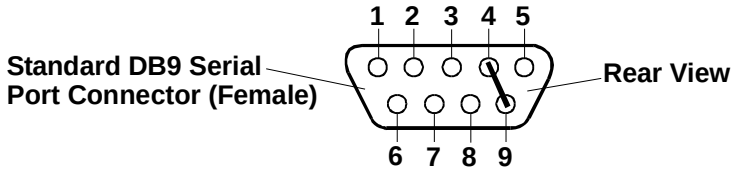

Figure 3-1. Oops! Jumper Serial Port (DB9)

Serial Console

The CoreModule 600 BIOS supports the serial console (or console redirection) feature. This I/O function is provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Serial Console Setup

The serial console feature is implemented by entering the serial console settings in BIOS Setup Utility and connecting the appropriate serial cable (a standard null modem serial cable or "Hot Cable") between one of the serial ports (serial 1 or 2), and the serial terminal or a PC with communications software. Refer to Chapter 4, BIOS Setup for the connection procedure, the serial console option settings, and the settings for the serial terminal, or PC with communications software.

Hot (Serial) Cable

To convert a standard serial cable to a "Hot Cable", certain pins must be shorted together at the Serial port connector or on the DB9 connector. Short together the RTS (7) and RI (9) pins on either serial port DB9 connector as shown in Figure 3-2.

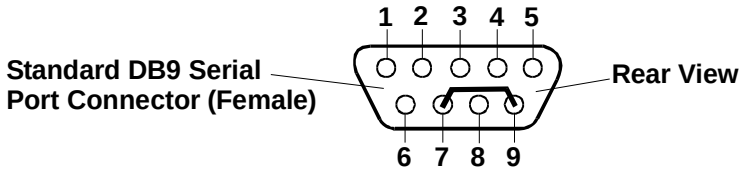

Figure 3-2. Serial Console Jumper

Watchdog Timer

The watchdog timer (WDT) restarts the system if a mishap occurs, ensuring proper start-up after the interruption. Possible problems include failure to boot properly, the application software's loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (watchdog timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the OS fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT in the Custom Configuration Screen of BIOS Setup. Set the WDT for a time-out interval in seconds, between 1 and 255, in one second increments. Ensure you allow enough time for the boot process to complete and for the OS to boot. The OS or application must tickle (turnoff) the WDT as soon as it comes up. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some Ampro Board Support Packages provide an API interface to the WDT. The application must tickle (turnoff) the WDT in the time set when the WDT is initialized or the system will be reset. You can use a BIOS call to tickle the WDT or access the hardware directly.

The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

- Watchdog Code examples – Ampro has provided source code examples on the CoreModule 600 Doc & SW CD-ROM illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file in the Miscellaneous Source Code Examples subdirectory, under the CoreModule 600 Software menu on the CoreModule 600 Doc & SW CD-ROM.

Power Interface (J6)

The CoreModule 600 SBC requires one +5 volt power source and uses a 10-pin header with 0.100" spacing. When the +5 power drops below ~ 4.63V, a low voltage reset triggers a system interrupt. The power input connector (J6) supplies the voltages listed in Table 3-19 directly to the module:

Table 3-19 gives the signals and descriptions for each pin and Table 3-20 gives the pin arrangement.

Table 3-19. Power Interface Pins/Signals (J6)

Pin #	Signal	Description
1	GND	Ground
2	+5V	+5 volts
3	Key	Key pin (Ground at board)
4	+12V	+12 volts routed to PC/104 and PC/104-Plus connectors
5	GND	-5 volts (Not used)
6	+3.3V	+3.3 volts routed to PC/104-Plus connector
7	GND	Ground
8	+5V	+5 volts
9	GND	Ground
10	+5V	+5 volts

Note: The shaded area denotes power or ground.

Table 3-20. Power Interface Pin Arrangement (J6)

Pin #	Signal	Pin #	Signal
1	GND	2	+5
3	Key	4	+12
5	GND	6	+3.3V
7	GND	8	+5
9	GND	10	+5

Note: The shaded area denotes power or ground.

Chapter 4 BIOS Setup

Introduction

This chapter describes the BIOS Setup menus and the various screens used for configuring the CoreModule 600. Some features in the Operating System or application software may require configuration in the BIOS Setup screens.

This section assumes the user is familiar with general BIOS Setup and does not attempt to describe the BIOS functions. Refer to the appropriate PC reference manuals for information about the software interface of the onboard ROM-BIOS. If Ampro has added to or modified the standard functions, these functions will be described.

The options provided for the CoreModule 600 are controlled by BIOS Setup. BIOS Setup is used to configure the module, modify the fields in the Setup screens, and save the results in the onboard configuration memory. Configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and the flash memory.

The Setup information is retrieved from configuration memory when the module is powered up or when it is rebooted. Changes made to the Setup parameters, with the exception of the time and date settings, do not take effect until the module is rebooted.

Setup is located in the ROM BIOS and can be accessed, when prompted using the <Del> key, while the module is in the Power-On Self Test (POST) state, just before completing the boot process. The screen displays a message indicating when you can press <Del> to enter the BIOS Setup Utility.

The CoreModule 600 Setup Utility is used to configure items in the BIOS using the following menus:

- BIOS and Hardware Settings
- Reload Initial Settings
- Load Factory Default Settings
- Exit, Saving Changes
- Exit, Discarding Changes

Table 4-1 summarizes the list of BIOS menus and some of the features available for CoreModule 600. The BIOS Setup menu offers the menu choices listed above and the related topics and screens are described on the following pages.

Accessing BIOS Setup (VGA Display)

To access BIOS Setup using a VGA display for the CoreModule 600:

1. Turn on the VGA monitor and the power supply to the CoreModule 600.
2. Start Setup by pressing the [Del] key, when the following message appears on the boot screen.

```
Hit <Del> if you want to run SETUP
```

NOTE	If the setting for *Memory Test* is set to Fast, you may not see this prompt appear on screen if the monitor is too slow to display it on start up. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup.

3. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.
4. Follow the instructions at the bottom of each screen to navigate through the selections and modify any settings.

Accessing BIOS Setup (Serial Console)

Entering the BIOS Setup, in serial console mode, is very similar to the steps you use to enter BIOS Setup with a VGA display, except the settings and actual keys you use.

1. Set the serial terminal, or the PC with communications software to the following settings:
   - 115k baud
   - 8 bits
   - One stop bit
   - No parity
   - No hardware handshake
2. Connect the serial terminal, or the PC with serial terminal emulation, to one of the serial ports, Serial Port 1 or 2, of the CoreModule 600.
   - If the BIOS option, *Serial Console* is set to [Enable], use a standard null-modem serial cable.
   - If the BIOS option, *Serial Console* is set to [Hot Cable], use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.
3. Turn on the serial terminal, or the PC with serial terminal emulation, and the power supply to the CoreModule 600.
4. Start Setup by pressing the Ctl–c keys, when the following message appears on the boot screen.

```
Hit ^C if you want to run SETUP
```

5. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.

NOTE	The serial console port is not hardware protected, and is not listed in the COM table within BIOS Setup. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

Table 4-1. BIOS Setup Menus

BIOS Setup Menu	Item/Topic
BIOS and Hardware Settings	Date and Time Drive Assignment Boot Order Drive and Boot Options Keyboard & Mouse (settings) User Interface (options) Memory (settings) Power Management Advanced Features On-Board Features (Serial, Parallel, USB, Video, etc.) PCI (options) Plug and Play (options)
Reload Initial Settings	Resets the BIOS (CMOS) to the most recent settings
Load Factory Default Settings	Resets BIOS (CMOS) to factory settings
Exit, Saving Changes	Writes all changes to BIOS (CMOS) and exits
Exit, Discarding Changes	Closes BIOS without saving changes except time and date

BIOS Menus

BIOS Setup Opening Screen

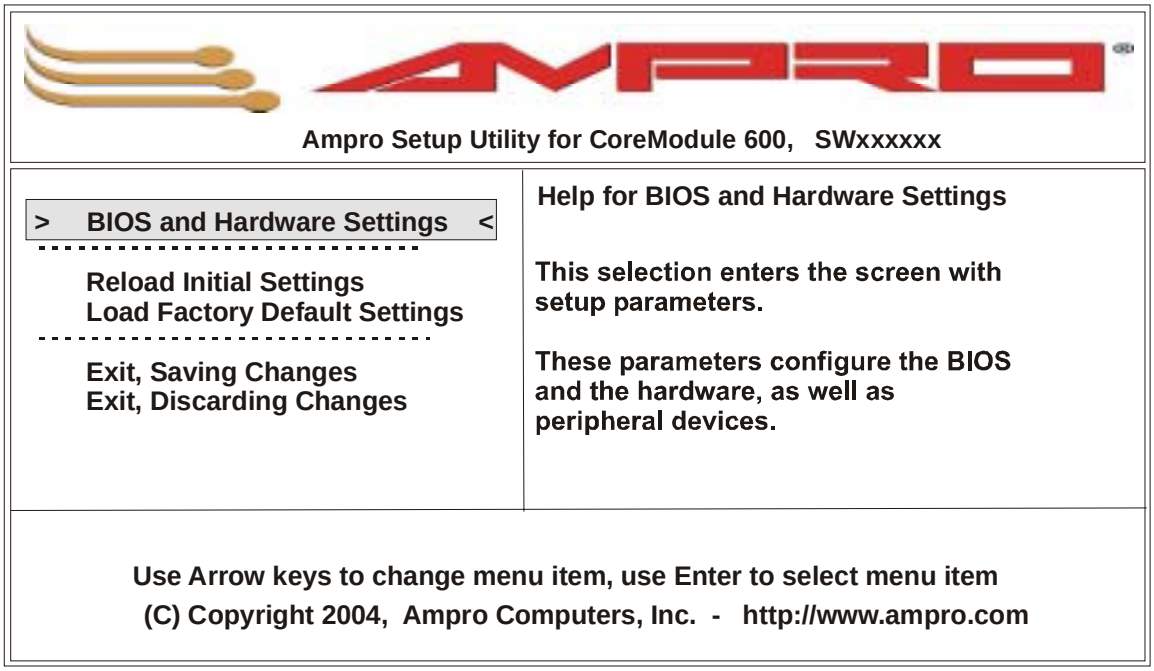

Figure 4-1. Opening BIOS Screen

NOTE	For the most current BIOS Information, refer to the Hardware Release Notes provided as hard copy in the shipping container.

NOTE	The default values or the typical settings are shown highlighted (**bold text**) in the list of options on the following pages. Refer to the bottom of the BIOS screens for navigation instructions and when making selections.

BIOS Configuration Screen

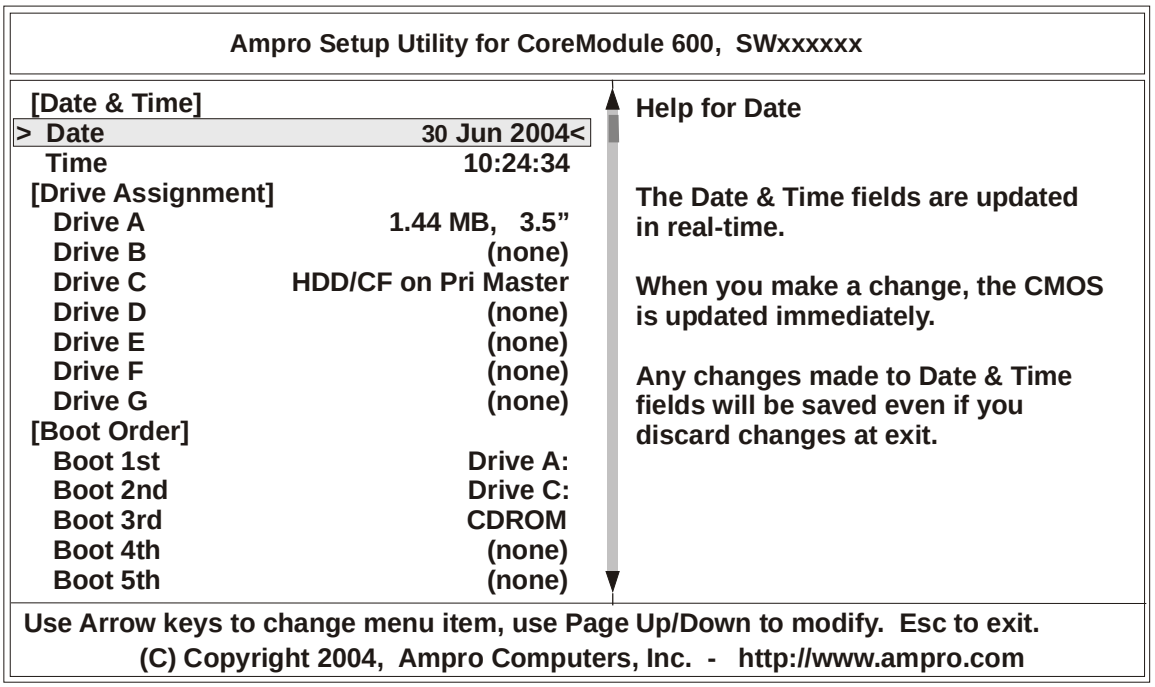

Figure 4-2. Modifying Setup Parameters Screen

- **Date & Time**
  - DATE (dd:mmm:yyyy) – This field requires the alpha-numeric entry of the calendar month, day of the month, and all 4 digits of the year to indicate the century plus year (*15 Jun 2004*).
  - Time (hh:mm:ss) – This requires 24 hour Clock setting in hours, minutes, and seconds
- **Drive Assignments**
  - Drive A – [none], [360kB, 5.25”], [1.2MB, 5.25”], [720kB, 3.5”], [**1.44MB, 3.5”**], [2.88MB, 3.5”], or [USB Floppy]

NOTE	If USB Boot Support is [Disabled], the USB Floppy selections are invalid and Drive B must be set to [none]. See Table 4-2 Floppy Drive Setting.

  - Drive B – [**none**], [360kB, 5.25”], [1.2MB, 5.25”], [720kB, 3.5”], [1.44MB, 3.5”], [2.88MB, 3.5”], or [USB Floppy]

NOTE	If a CompactFlash device is used in the system, it is always configured as [HDD/CF Pri Master or Salve].

  - Drive C – [none], [**HDD/CF on Pri Master**], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [USB HDD], or [USB CDROM]
  - Drive D – [**none**], [HDD/CF on Pri Master], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [USB HDD], or [USB CDROM]
  - Drive E – [**none**], [HDD/CF on Pri Master], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [USB HDD], or [USB CDROM]

Table 4-2. Floppy Drive BIOS Settings

# of Floppy Drive(s)	BIOS Settings
None	• Set Drives A and B to [None]
(1) Non-USB Floppy*	• Configure Drive A to floppy drive type (For example, [1.44MB, 3.5"]) • Set Drive B to [None]
(1) USB Floppy	• Set USB Boot Support to [Enable] • Set Drive A to [USB Floppy] • Set Drive B to [None]
(2) Floppy drives (1 USB Floppy and 1 non-USB Floppy drive*)	• Set USB Boot Support to [Enable] • Configure Drive A to floppy drive type (For example, [1.44MB, 3.5"]) • Set Drive B to [USB Floppy]

- **Table Note:** *A standard 34-pin floppy cable has a twist in the cable wiring between the Floppy A and B connectors, where Floppy B has the straight through cable (non-twist) and is the middle connector. Due to the CoreModule 600's configuration, the physical Floppy A connector is not accessible, so you must connect a standard floppy drive to the Floppy B connector on the cable.
- Drive F – [**none**], [HDD/CF on Pri Master], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [USB HDD], or [USB CDROM]
- Drive G – [**none**], [HDD/CF on Pri Master], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [USB HDD], or [USB CDROM]

- **Boot Order**
  - Boot 1st – [none], [**Drive A**], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
  - Boot 2nd – [none], [Drive A], [Drive B], [**Drive C**], [Drive D], [CDROM], [Alarm], or [Reboot]

NOTE The [Alarm] option sounds beeps on the PC speaker and can be listed, like [Reboot], as the last boot device to indicate no bootable device was found.

Any drive can be listed as a boot drive.

- Boot 3rd – [none], [Drive A], [Drive B], [Drive C], [Drive D], [**CDROM**], [Alarm], or [Reboot]
- Boot 4th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
- Boot 5th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
- Boot 6th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]

NOTE The default Boot order is, A, C, CD-ROM, and the BIOS will start its search for a bootable device in drive A, then C, then CD-ROM. If no bootable device is found and [Reboot] was not selected as an option, the screen will display "No Bootable Device Available" and the boot process will stop, allowing you to select from:

R – for Reboot, or
S – for Setup.

If you do not choose R or S, the boot process stops until you intervene, unless you have selected [Reboot] as an Boot order option.

- **Drive and Boot Options**
  - Floppy over Parallel – [Disabled] or [**Enabled**]
    - If [Enabled], this options selects the Floppy Drive instead of the Parallel port on the shared connector.
    - If [Disabled], this options selects the Parallel port instead of the Floppy Drive on the shared connector.
  - Floppy Seek – [**Disabled**] or [Enabled]
  - Hard disk Seek – [**Disabled**] or [Enabled]
  - Boot Method – [**Boot Sector**] or [Windows CE]

    Boot Sector is the traditional method for booting the system. If [Windows CE] is selected, the BIOS attempts to load the NK.BIN file from the root directory of each boot device.
  - Primary IDE Cable – [**Auto**], [40 Wire], or [80 Wire]

    Setting these fields to [Auto], causes the BIOS to query the attached IDE device to determine the type of IDE cable used. If the BIOS detects [40 wire], or you select it, the BIOS will not use UDMA-66 or faster mode when sending signals to/from the IDE device.
- **Keyboard and Mouse** (Configuration)
  - Numlock – [**Disabled**] or [Enabled]
  - Typematic – [Disabled] or [**Enabled**]

    This field is used for the keyboard.
  - Delay – [**250ms**], [500ms], [750ms], or [1000ms]

    This field is used for the keyboard and determines how many milliseconds the keyboard controller waits before stating to repeat a key, if the key is held down on the keyboard.
  - Rate – [**30cps**], [24cps], [20cps], [15cps], [12cps], [10cps], [8cps], or [6cps]

    This is a keyboard field and determines the rate, in characters per second, the keyboard controller will repeat a key, if the key is held down on the keyboard.
  - Initialize PS/2 Mouse – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the BIOS will initialize the PS/2 mouse.

    If the PS/2 mouse is [Disabled], then the BIOS will not initialize the PS/2 mouse, which may not be recognized by the Operating System.
- **User Interface**
  - Show "Hit <Del>…" – [Disabled] or [**Enabled**]

    This field, if Enabled, will place "Hit Del" on screen during the boot process, to indicate when you may press "Del" to enter the BIOS Setup menus.
  - F1 Error Wait – [**Disabled**] or [Enabled]

    If this field is [Enabled], the BIOS will display an Error message indicating when an error has occurred during POST (power on self test) and wait for you to respond by hitting the F1 key.

    If [Disabled], and an error occurs during POST, the BIOS will attempt to continue the boot process.
  - Config Box – [Disabled] or [**Enabled**]

    This field, if Enabled, displays the Configuration Summary Box, which list all of the configuration information for the system, at the completion of POST, but before the Operating System is loaded.

- Splash Screen – [**Disabled**] or [Enabled]
  - If Splash Screen is [Enabled] it stays on screen, until the booted Operating System changes it, if the Config Box option is Disabled.
  - If Config Box option is [Enabled], the Splash Screen stays on screen until the Config Box is displayed.

  The Splash Screen is a graphical image displayed as the default (Ampro Splash Screen) or a user customized image on screen. Refer to the Splash Screen Customization topic later in this chapter for instructions on how to customize the splash screen.

- **Memory**
  - Memory Test – [**Fast**], [Standard], or [Exhaustive]
    - If this field is set to [Fast], only basic memory tests are performed during POST to shorten POST time.
    - If this field is set to [Standard], more than basic tests are performed, but POST time is increased.
    - If this field is set to [Exhaustive], more rigorous tests are performed on memory, but this takes a significant amount of time for POST to complete.
  - Memory Hole – [**Disabled**], [1MB], or [2MB]

    This field specifies the size of an optional memory hole, below 16MB. Access to the memory addresses inside the memory hole region are forwarded to the PC/104 bus, where memory mapped PC/104 devices have access.
  - Shadow D000-D3FF – [**Disabled**] or [Enabled]

    These Shadow fields specify if BIOS option ROMs in the indicated segments should be shadowed to RAM. Shadowing option ROMs can potentially speed up the operation of the system. The indicated segments are only for option ROMs present on add-on PC/104 and PC/104-Plus cards.
  - Shadow D400-D7FF – [**Disabled**] or [Enabled]
  - Shadow D800-DBFF – [**Disabled**] or [Enabled]
  - Shadow DC00-DFFF – [**Disabled**] or [Enabled]

- **Power Management**
  - ACPI – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the Advanced Configuration and Power Interface API is turned on.
  - APM – [**Disabled**] or [Enabled]

    If this field is set to [Enabled], the Advanced Power Management API is turned on.

- **Advanced features**
  - Post Memory Manager – [**Disabled**] or [Enabled]

    If this field is set to [Enabled], the Post Memory Manger API is turned on. The Post Memory Manger can be used by BIOS option ROMs to allocate memory in a well defined way.
  - CPU Serial Number – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the internal serial number in the Intel CPU is accessible by the Operating System and/or Applications that can make use of this information.

- Watchdog Timeout (sec) – [select whole number between 1 and 255 seconds, in 1 second increments] or [**Disabled**]

  If this field is enabled by selecting a time interval (1 to 255 seconds), will direct the watchdog timer to reset the system if it fails to boot the OS properly. Refer to the watchdog timer section in Chapter 3 for more information.

- Serial Console – [**Hot Cable**] or [Enabled]

  - The Hot Cable option only allows console redirection when a Hot Cable is actually connected to COM 1 or 2. Use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.
  - The [Enabled] option instructs the BIOS to operate in the console redirection mode at all times with the serial port selected in the Serial Console > Port field listed below. Use a standard null-modem serial cable.
  - However, connecting a Hot Cable to the other port (port not selected) overrides the setting of this field [Enabled] and the Serial Console > Port field.

  - Port – [**3F8h**], [2F8h], [3E8h], or [2E8h]

    This field selects the Serial (COM) port address used for console redirection when [Enabled] has been selected in Serial Console. Use a standard null-modem serial cable.

    However, connecting a Hot Cable to the other port (port not selected) overrides this field setting and activates the connected port. Connecting a Hot Cable to one of the serial ports only allows console redirection when a Hot Cable is actually connected to Serial 1 or 2. Use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.

- **On-Board Serial Ports**

NOTE	Serial Ports 1 and 2 can not share the same IRQs, and the IRQs used for Serial Ports 1 and 2 can not be used for other devices and vice versa.

- Serial 1 – [Disabled], [**3F8h**], [2F8h], [3E8h], [2E8h], [260h], [2F0h], [3E0h], [2E0h], [200h], or [220h]

  This field specifies the base address used for Serial Port 1.

  - IRQ – [none], [1], [3], [**4**], [5], [6], [7], [9], [10], [11], [12], [14], or [15]

    This field specifies the IRQ used for Serial Port 1. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

  - Mode – [**RS-232**] or [RS-485]

    This field specifies the signal mode, RS232, or RS485, used for Serial Port 1. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

- Serial 2 – [Disabled], [3F8h], [**2F8h**], [3E8h], [2E8h], [260h], [2F0h], [3E0h], [2E0h], [200h], or [220h]

  This field specifies the base address used for Serial Port 2.

  - IRQ – [none], [1], [**3**], [4], [5], [6], [7], [9], [10], [11], [12], [14], or [15]

    This field specifies the IRQ used for Serial Port 2. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

- **On-Board LPT Port**

  If the Floppy Drive is selected instead of the Parallel port, these settings have no effect.

  - LPT 1 – [Disabled], [**378h**], [278h], [3BCh], [370h], or [270h]

    This field specifies the base address used for the Parallel Port (LPT1)

    - IRQ – [none], [1], [3], [4], [5], [6], [**7**], [8], [9], [10], [11], or [12]
    - DMA – [**3**], [2], [1], or [0]
    - Mode – [**Standard**], [SPP (bi-dir)], [EPP 1.9 + SPP], [EPP 1.7 + ECP], [EPP 1.9 + ECP], or [ECP]

      This field specifies the Mode used for the Parallel Port (LPT1).

- **On-Board Controllers**

  - Ethernet Controller – [Disabled] or [**Enabled**]
    - If this field is set to [Enabled], the Ethernet controller is available to support the Ethernet port (J9) on the board.
  - Primary IDE – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], then the on-board Primary IDE controller is used.
  - PS/2 Mouse – [Disabled] or [**Enabled**]
    - If this field is set to [Enabled], then the on-board PS/2 Mouse controller is used and assigned an IRQ by the BIOS, typically IRQ 12.
    - If this field is set to [Disabled], then the on-board PS/2 Mouse controller is not used and IRQ 12 is available for other devices.
  - USB – [Disabled] or [**Enabled**]
    - If this field is set to [Enabled], the USB controller is available to support the two USB ports provided through the Utility connector (J5).

- **On-Board Video**

  - Framebuffer Size – [Disabled], [**8MB**], [16MB], or [32MB]

    This field specifies the amount of system memory used for the on-board Video Framebuffer. The amount of memory used for the Framebuffer of the on-board Video controller is subtracted from the available system memory.
  - AGP Aperture Size – [2MB], [4MB], [8MB], [16MB], [32MB], [64MB], [**128MB**], or [256MB]

    This field specifies the size of memory used for the AGP Aperture. The AGP Aperture Size indicates the amount of system memory that can be used for the 3D engine. The system memory is still available for the system use, unless an application actually uses the AGP Aperture memory.
  - Display – [**CRT**], [LCD], [LCD + CRT]

    This field specifies the display type used.
    - If [LCD] or [CRT+LCD] is selected, the panel type selection indicates the configuration the LCD panel attached. See the next field and Table 4-2.
    - If the [CRT+LCD] is selected, the same video information is shown on both displays simultaneously.

- Panel Type – [**640 x 480 x 18 TFT**]

  Refer to Table 4-2 for the list of supported resolutions and flat panel types. Some LCD panels may require video BIOS modifications. It you think this is the case, or would like help in setting up your LCD panel, contact Ampro for assistance with the LCD panel adaptation.

Table 4-2. LCD Panel Type List

#	LCD Resolution	LCD Type
1	**640 x 480 x 18 (bit)**	**TFT**
2	Reserved (Customer specific)	
3	Reserved (Customer specific)	
4	Reserved (Customer specific)	
5	640 x 480 x 16 (bit)	DSTN
6	Reserved (Customer specific)	
7	Reserved (Customer specific)	
8	Reserved (Customer specific)	

#	LCD Resolution	LCD Type
9	Reserved (Customer specific)	
10	800 x 600 x 18 (bit)	TFT
11	1024 x 768 x 18 (bit)	TFT
12	1280 x 1024 x 18 (bit)	TFT
13	Reserved (Customer specific)	
14	Reserved (Customer specific)	
15	1024 x 768 x 16 (bit)	DSTN
16	1280 x 1024 x 16 (bit)	DSTN

- **PCI**
  - INTA IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
  - INTB IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]
  - INTC IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]
  - INTD IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]
- **Plug and Play**
  - PnP BIOS – [Disabled] or [**Enabled**]
    - If this field is set to [Enabled], the BIOS uses Plug and Play adapter initialization and assigns the resources, such as I/O addresses, IRQs, and DMA channels to Plug and Play compatible devices. The resources assigned by the BIOS are based on the settings of the IRQ and DMA channel assignments listed in the following fields.
    - If this field is set to [Disabled], the IRQs and DMA channels listed below can not be assigned to Plug and Play devices.
  - PnP OS – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the BIOS makes the Plug and Play API available for Plug and Play Operating Systems. This allows the Plug and Play OS to get the Plug and Play information by calling the Plug and Play API.
  - Assign IRQ 1 – [**Disabled**] or [Enabled]
    - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
    - If another device in the system is using this IRQ, then this field should be set to [Disabled].
  - Assign IRQ 3 – [Disabled] or [**Enabled**] (Typically COM2)
    - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
    - If another device in the system is using this IRQ, then this field should be set to [Disabled].

- Assign IRQ 4 – [Disabled] or [**Enabled**] (Typically COM1)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 5 – [Disabled] or [**Enabled**]
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 6 – [**Disabled**] or [Enabled] (Typically Floppy Disk)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 7 – [Disabled] or [**Enabled**] (Typically LPT1)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 9 – [Disabled] or [**Enabled**] (Typically unused)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 10 – [Disabled] or [**Enabled**] (Typically unused)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 11 – [Disabled] or [**Enabled**] (Typically ISA Bridge/Native IDE)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 12 – [**Disabled**] or [Enabled] (Typically PS/2 Mouse)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 14 – [**Disabled**] or [Enabled] (Typically Hard Disk)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.

- If another device in the system is using this IRQ, then this field should be set to [Disabled].

♦ Assign IRQ 15 – [**Disabled**] or [Enabled] (Typically Hard Disk)

- If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
- If another device in the system is using this IRQ, then this field should be set to [Disabled].

♦ Assign DMA 0 – [**Disabled**] or [Enabled]

- If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
- If another device in the system is using this DMA channel, then this field should be set to [Disabled].

♦ Assign DMA 1 – [**Disabled**] or [Enabled]

- If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
- If another device in the system is using this DMA channel, then this field should be set to [Disabled].

♦ Assign DMA 2 – [**Disabled**] or [Enabled]

- If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
- If another device in the system is using this DMA channel, then this field should be set to [Disabled].

♦ Assign DMA 3 – [Disabled] or [**Enabled**]

- If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
- If another device in the system is using this DMA channel, then this field should be set to [Disabled].

♦ Assign DMA 5 – [Disabled] or [**Enabled**]

- If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
- If another device in the system is using this DMA channel, then this field should be set to [Disabled].

♦ Assign DMA 6 – [Disabled] or [**Enabled**]

- If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
- If another device in the system is using this DMA channel, then this field should be set to [Disabled].

♦ Assign DMA 7 – [Disabled] or [**Enabled**]

- If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
- If another device in the system is using this DMA channel, then this field should be set to [Disabled].

Splash Screen Customization

The CoreModule 600 BIOS supports a graphical splash screen, which can be customized by the user and displayed on screen when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image displayed on screen during the boot process and remain there, depending on the options selected in BIOS Setup, while the OS boots.

Splash Screen Image Requirements

The user's image may be customized with any bitmap software editing tool, but must be converted into an acceptable format with the tools (files and utilities) provided by Ampro. If the custom image is not converted with the utilities provided, then the image will not display properly when this field is selected in BIOS Setup.

NOTE	Do not use other splash screen conversion tools, as these will render an image that is not compatible with the CoreModule 600 BIOS.

The splash screen image supported by the CoreModule 600 BIOS should be:

- Bitmap image
- Exactly 640x480 pixels
- Exactly 16 colors
- A converted file size of not greater than 55kB

Converting the Splash Screen File

The following files are provided by Ampro on the CoreModule 600 Doc & SW CD-ROM and are required for converting a custom splash screen file. Refer to the CD-ROM for the utilities and an example of how to load a custom image in the *cm600\software\examples\splash* directory.

- splash.bmp
- convert.exe
- convert.idf
- resplash.com
- cm600.bin

The process of converting and loading a custom image onto the CoreModule 600 involves the following sequence of events:

- Prepare directory for conversion (create directory and copy files into it)
- Obtain the CoreModule 600 BIOS binary
- Prepare the custom image file
- Convert the image to an acceptable BIOS format
- Merge the image with BIOS binary to create new BIOS binary
- Load the new BIOS binary onto the CoreModule 600

NOTE	You can use any Windows PC to convert the custom image, but your PC must have an internet browser to access, view, and make selections in the main menu of the CoreModule 600 Doc & SW CD-ROM. For example: Microsoft Internet Explorer 4.x, or greater, Netscape Navigator version 4.x, or greater, or the equivalent.

Use the following steps to convert and load your custom image onto the CoreModule 600.

1. Copy the files from the *CM600\software\examples\splash* directory on the CD-ROM to a new directory (conversion directory) on your PC.

   This new conversion directory is where you intend to do the conversion and save the file.

2. Ensure you remove the read-only attributes from all the files as part of the file copying process.

3. Copy the CoreModule 600 BIOS binary file (cm600.bin) to the new conversion directory on your PC where the other files and utilities are located.

   If this file is not on the CoreModule 600 Doc & SW CD-ROM, you will have to obtain it from Ampro.

NOTE	Ampro recommends keeping a copy of this original cm600.bin file, just in case you encounter problems with your new file or have difficulty updating the BIOS with the new image.

4. Prepare your custom image file with any Windows bitmap software editing tool.

   - For example, Corel Photo-Paint, Adobe Photoshop, or the Windows Paint program provided with Windows. You can insert a desired graphic image, logo, text, etc. into the file.
   - The custom image must be a bitmap image in .bmp format at 640x480 pixels and it must be 16 colors. The file should be about 153,718 bytes. Refer to the example file splash.bmp.

5. Save your custom image file as splash.bmp at 640x480 pixels by 16 colors.

   - If your custom image file is not approximately 153,718 bytes in size it is probably not in the right format or is too complex to be used in the BIOS. You will have to edit it down in size until you have reached an acceptable file size.
   - If you are doubtful about the conversion process, due to the file size, Ampro recommends making a copy of your new splash.bmp, so that you can edit it later if the conversion does not yield a small enough file. Otherwise, you may have to re-create your custom image before you can edit it down to an acceptable file size.

6. If your custom image file is not on the conversion PC, copy the new splash.bmp file to the conversion directory.

7. Run the following command from DOS, or a Windows DOS pop-up screen to convert your new splash.bmp file.

   ```
   C:\splash>convert convert.idf
   ```

   This conversion should yield a *splash.rle* file of approximately 55kB in size or less, depending on the complexity of your image.

8. If the splash.rle file size is greater than 55kB, go back to the unconverted image file and edit the file.

   You may reduce the file size of the converted image (splash.rle) by reducing the image's complexity.

9. Run the following command to merge the converted image with the BIOS binary file.

   ```
   C:\splash>resplash cm600.bin splash.rle cm600n.bin
   ```

   This creates a new BIOS named cm600n.bin, which has the new splash image. This new BIOS is ready to be loaded onto the CoreModule 600.

10. Copy the files update.bat, aflash.exe, and cm600n.bin to a DOS boot floppy.

11. Boot the CoreModule 600 from the floppy and run update.bat.

12. Cycle the power to the CoreModule 600 and enter BIOS Setup to enable the splash screen.

Appendix A Technical Support

Ampro Computers, Inc. provides a number of methods for contacting Technical Support listed below in Table A-1. Requests for support through the Virtual Technician are given the highest priority, and usually will be addressed within one working day.

- Ampro Virtual Technician – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro web site at http://ampro.custhelp.com. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register and log in to access this service.

  Personal Assistance – You may also request personal assistance by going to the "Ask a Question" area in the Virtual Technician. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request you can go to the "My Stuff" area and log in to check status, update your request, and access other features.

- Embedded Design Resource Center – This service is also free and available 24 hours a day at the Ampro web site at http://www.ampro.com. However, you must login to access this service.

  The Embedded Design Resource Center was created as a resource for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience. This page contains links to White Papers, Specifications, and additional technical information.

Table A-1. USA Technical Support Contact Information

Method	Contact Information
Virtual Technician	http://ampro.custhelp.com
Web Site	http://www.ampro.com
Standard Mail	Ampro Computers, Incorporated 5215 Hellyer Avenue San Jose, CA 95138-1007, USA

Appendix B Connector Part Numbers

The following table provides the mating connector part numbers, and if applicable the ribbon-cable part numbers, used to mate to the referenced connectors on the CoreModule 600. All connectors use 0.100" (2.54mm) pin spacing unless otherwise indicated.

Table B-1. Connector and Manufacturer's Part Numbers

Connector	Pin Number/ Orientation	Manufacturer	Manufacturer's PN
J2 – IDE	40-pin	Molex	15-49-6402
J5 – Utility	80-pin	HIROSE	FX2BA-80S-1.27R
J6 – Power	10-pin	SAMTEC	SMH-15-02-S-D
J8 – Video	44-pin, 2mm	3M	Housing: 87044-1000
			Ribbon: 3625/44
J9 – Ethernet	10-pin	SAMTEC	SMH-15-02-S-D

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